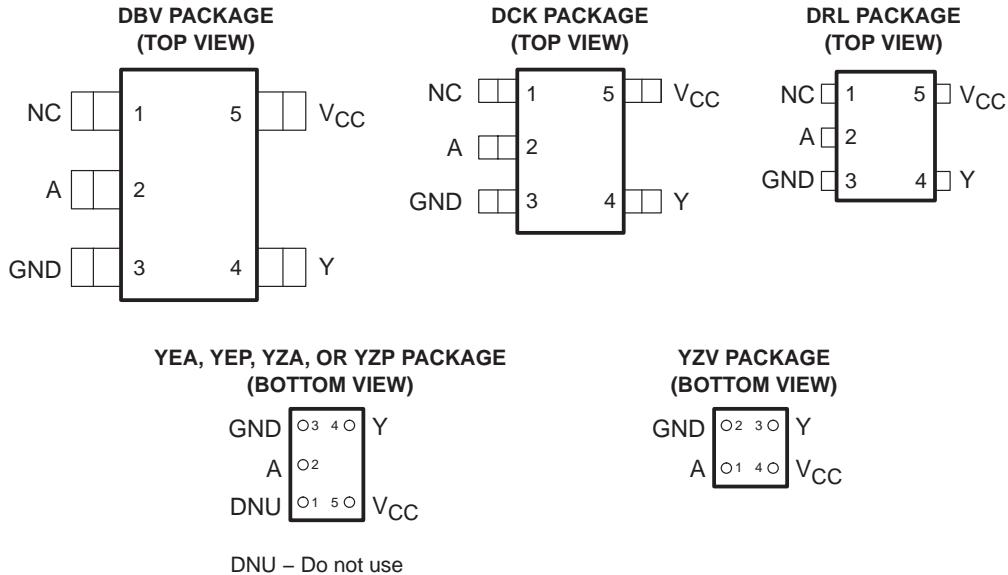


- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.6 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

description/ordering information

This single Schmitt-trigger inverter is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G14 device contains one inverter and performs the Boolean function $Y = \overline{A}$. The device functions as an independent inverter, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SN74LVC1G14

SINGLE SCHMITT-TRIGGER INVERTER

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ORDERING INFORMATION

TA	PACKAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING [‡]
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Reel of 3000	SN74LVC1G14YEAR
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		SN74LVC1G14YZAR
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LVC1G14YEPR
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G14YZPR
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZV (Pb-free)	Reel of 3000	SN74LVC1G14YZVR
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G14DBVR
	SOT (SC-70) – DCK	Reel of 250	SN74LVC1G14DBVT
		Reel of 3000	SN74LVC1G14DCKR
	SOT (SOT-533) – DRL	Reel of 250	SN74LVC1G14DCKT
		Reel of 4000	SN74LVC1G14DRLR
			CF_

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YEP, YZA/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic) (DBV, DCK, DRL, YEA, YEP, YZA, and YZP Package)



logic diagram (positive logic) (YZV Package)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DBV package	206°C/W
DCK package	252°C/W
DRL package	142°C/W
YEA/YZA package	154°C/W
YEP/YZP package	132°C/W
YZV package	TBD°C/W
Storage temperature range, T_{STG}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65$ V	-4	mA
		$V_{CC} = 2.3$ V	-8	
			-16	
		$V_{CC} = 3$ V	-24	
		$V_{CC} = 4.5$ V	-32	
I_{OL}	Low-level output current	$V_{CC} = 1.65$ V	4	mA
		$V_{CC} = 2.3$ V	8	
			16	
		$V_{CC} = 3$ V	24	
		$V_{CC} = 4.5$ V	32	
T_A	Operating free-air temperature	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{T+} Positive-going input threshold voltage		1.65 V	0.79	1.16		V
		2.3 V	1.11	1.56		
		3 V	1.5	1.87		
		4.5 V	2.16	2.74		
		5.5 V	2.61	3.33		
V _{T-} Negative-going input threshold voltage		1.65 V	0.39	0.62		V
		2.3 V	0.58	0.87		
		3 V	0.84	1.14		
		4.5 V	1.41	1.79		
		5.5 V	1.87	2.29		
ΔV _T Hysteresis (V _{T+} – V _{T-})		1.65 V	0.37	0.62		V
		2.3 V	0.48	0.77		
		3 V	0.56	0.87		
		4.5 V	0.71	1.04		
		5.5 V	0.71	1.11		
V _{OH}	I _{OH} = –100 μA	1.65 V to 4.5 V	V _{CC} – 0.1			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.9			
	I _{OH} = –16 mA		2.4			
	I _{OH} = –24 mA		2.3			
	I _{OH} = –32 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 100 μA	1.65 V to 4.5 V		0.1		V
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 8 mA	2.3 V		0.3		
	I _{OL} = 16 mA		0.4			
	I _{OL} = 24 mA		0.55			
	I _{OL} = 32 mA	4.5 V	0.55			
I _I	A input	V _I = 5.5 V or GND	0 to 5.5 V		±5	μA
I _{off}		V _I or V _O = 5.5 V	0		±10	μA
I _{CC}	V _I = 5.5 V or GND,	I _O = 0	1.65 V to 5.5 V		10	μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		3 V to 5.5 V		500	μA
C _i	V _I = V _{CC} or GND		3.3 V		4.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 5 V ± 0.5 V	UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2.8	9.9	1.6	5.5	1.5 4.6 0.9 4.4 ns

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switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.8	11	2	6.5	1.8	5.5	1.2	5	ns

operating characteristics, $T_A = 25^\circ\text{C}$

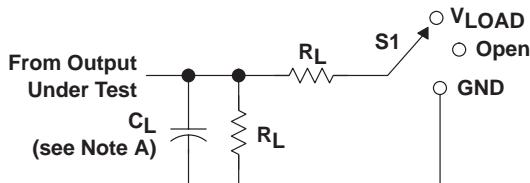
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$		$V_{CC} = 2.5 \text{ V}$		$V_{CC} = 3.3 \text{ V}$		$V_{CC} = 5 \text{ V}$		UNIT
		TYP		TYP		TYP		TYP		
C_{pd} Power dissipation capacitance	$f = 10 \text{ MHz}$		20		21		22		25	pF

SN74LVC1G14

SINGLE SCHMITT-TRIGGER INVERTER

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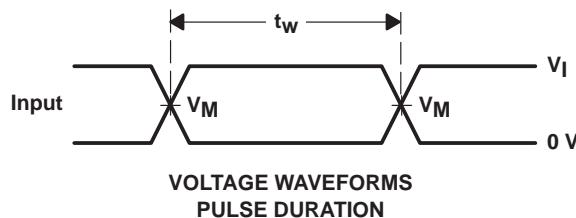
PARAMETER MEASUREMENT INFORMATION



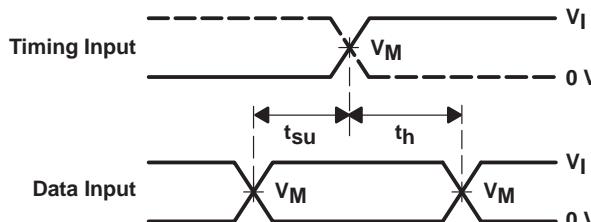
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

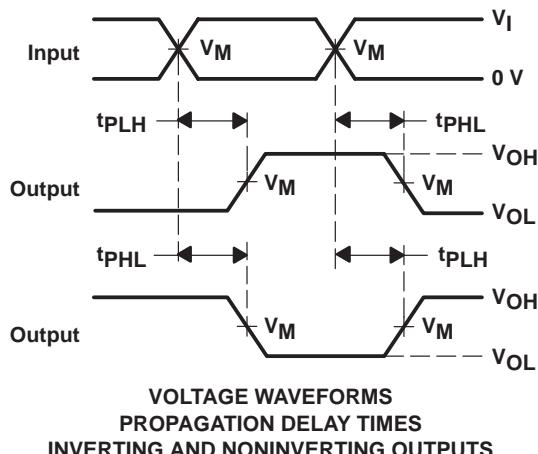
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 V \pm 0.15 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1 M\Omega$	0.15 V
$2.5 V \pm 0.2 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1 M\Omega$	0.15 V
$3.3 V \pm 0.3 V$	3 V	≤ 2.5 ns	1.5 V	6 V	15 pF	$1 M\Omega$	0.3 V
$5 V \pm 0.5 V$	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1 M\Omega$	0.3 V



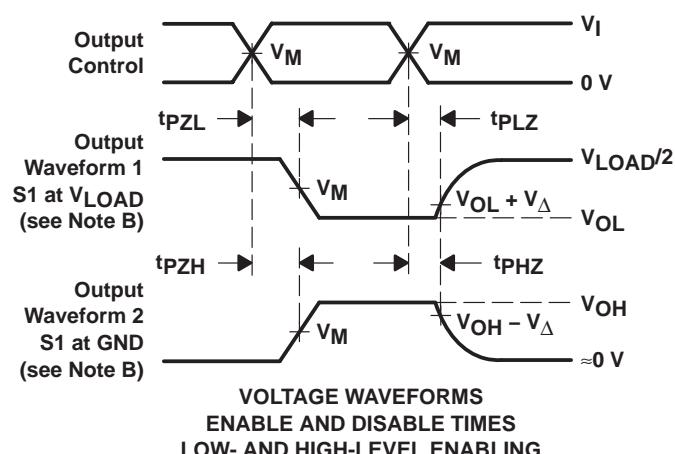
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



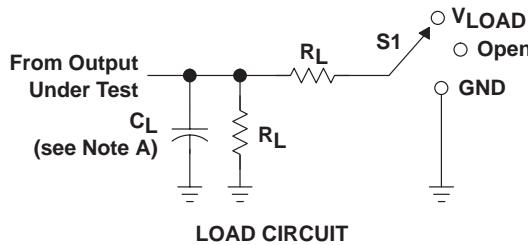
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

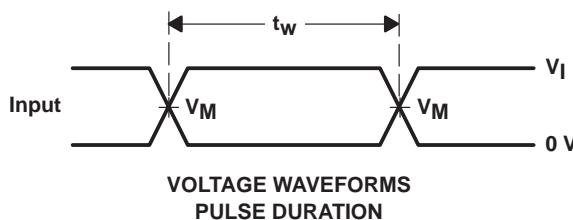
PARAMETER MEASUREMENT INFORMATION



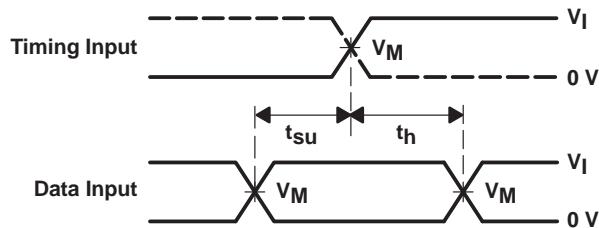
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

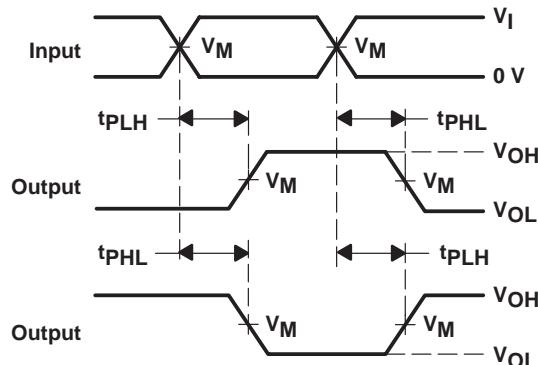
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 V \pm 0.15 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.2 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3 V \pm 0.3 V$	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5 V \pm 0.5 V$	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



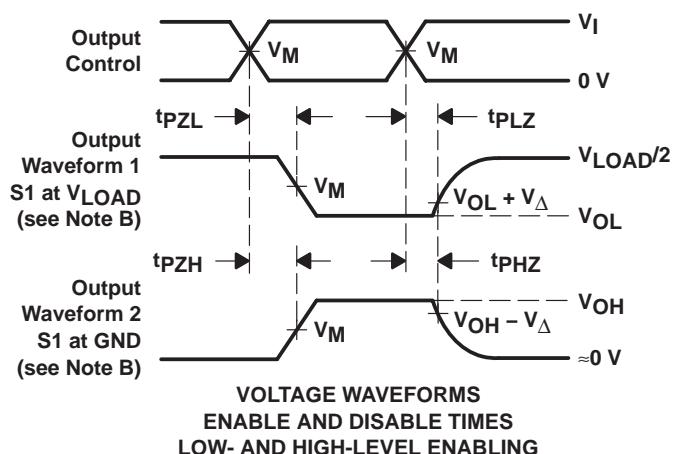
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
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NOTES:

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- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC1G14DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DBVT	ACTIVE	SOT-23	DBV	5	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DBVTE4	ACTIVE	SOT-23	DBV	5	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14YEAR	ACTIVE	WCSP	YEA	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G14YEPR	ACTIVE	WCSP	YEP	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G14YZAR	ACTIVE	WCSP	YZA	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1G14YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

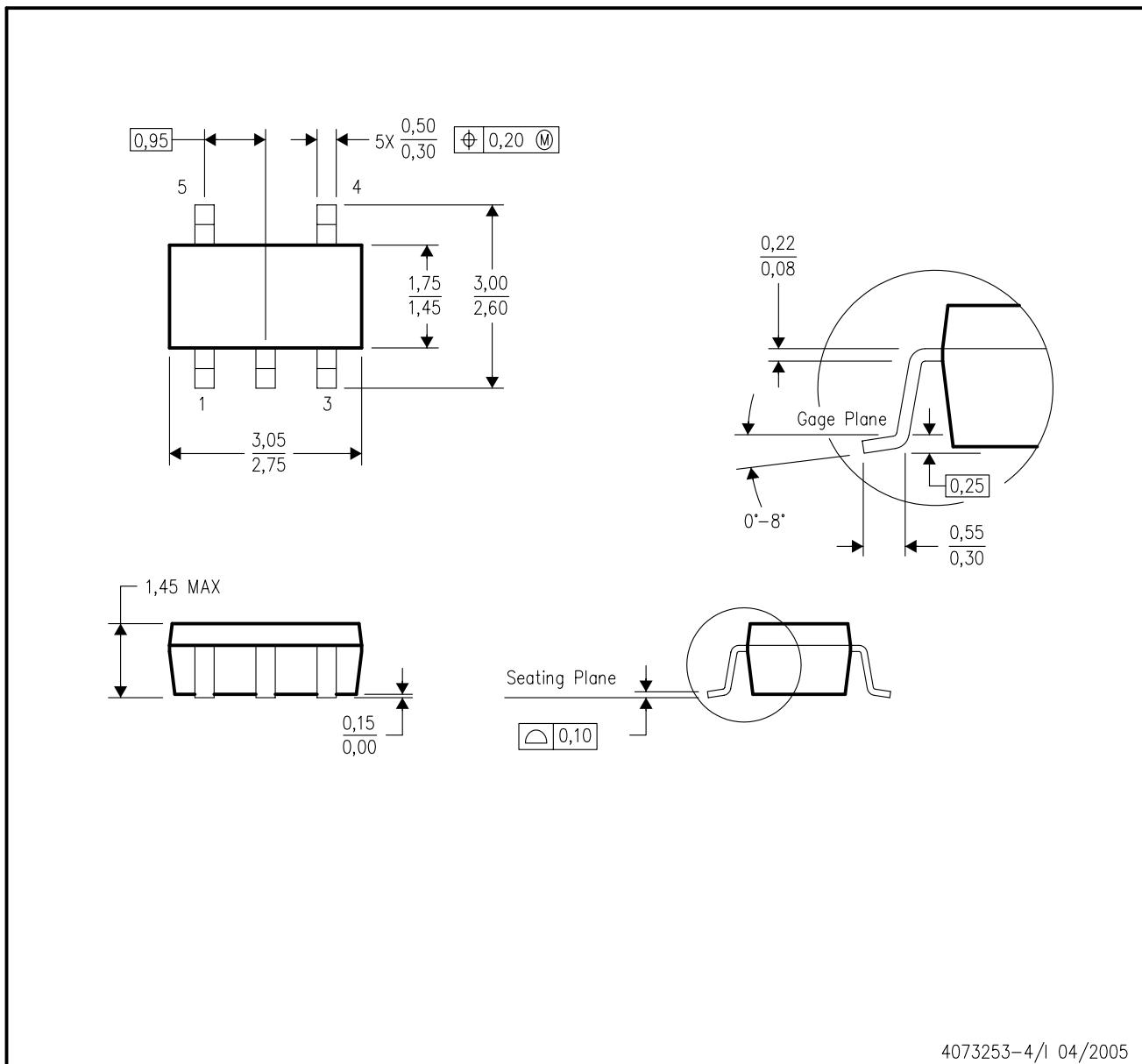
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DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



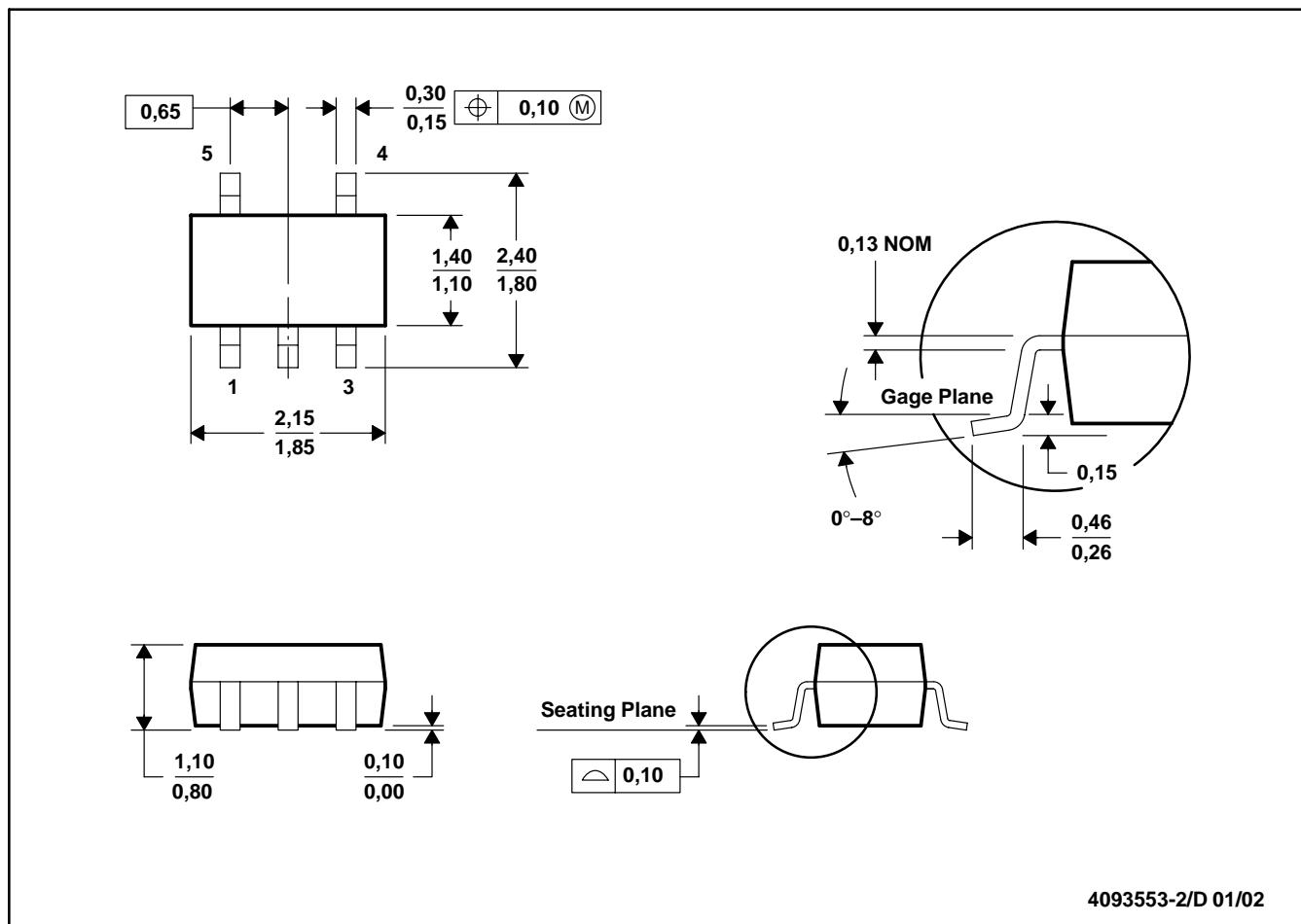
4073253-4 / 04/2005

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion.
- Falls within JEDEC MO-178 Variation AA.

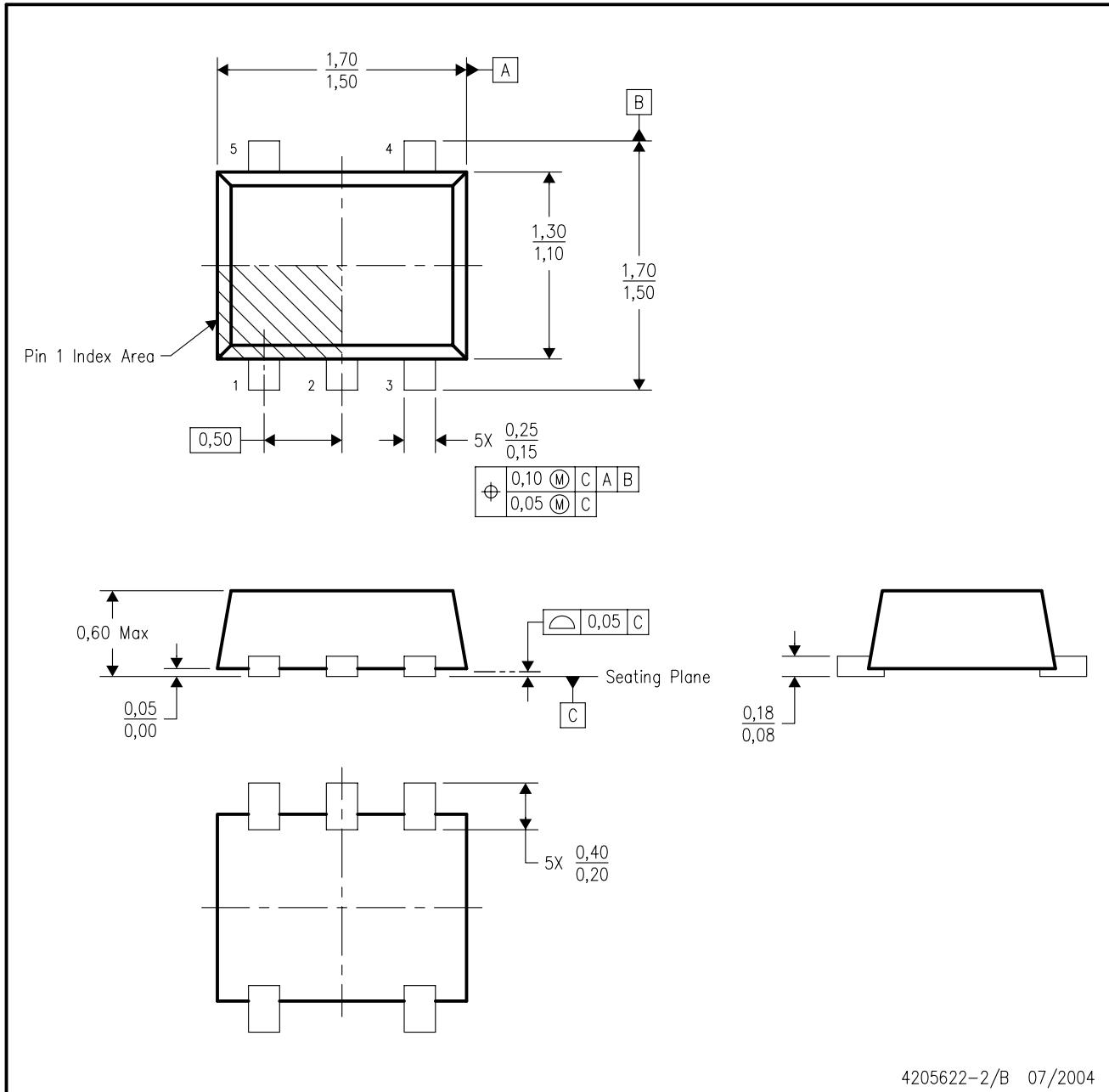
DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

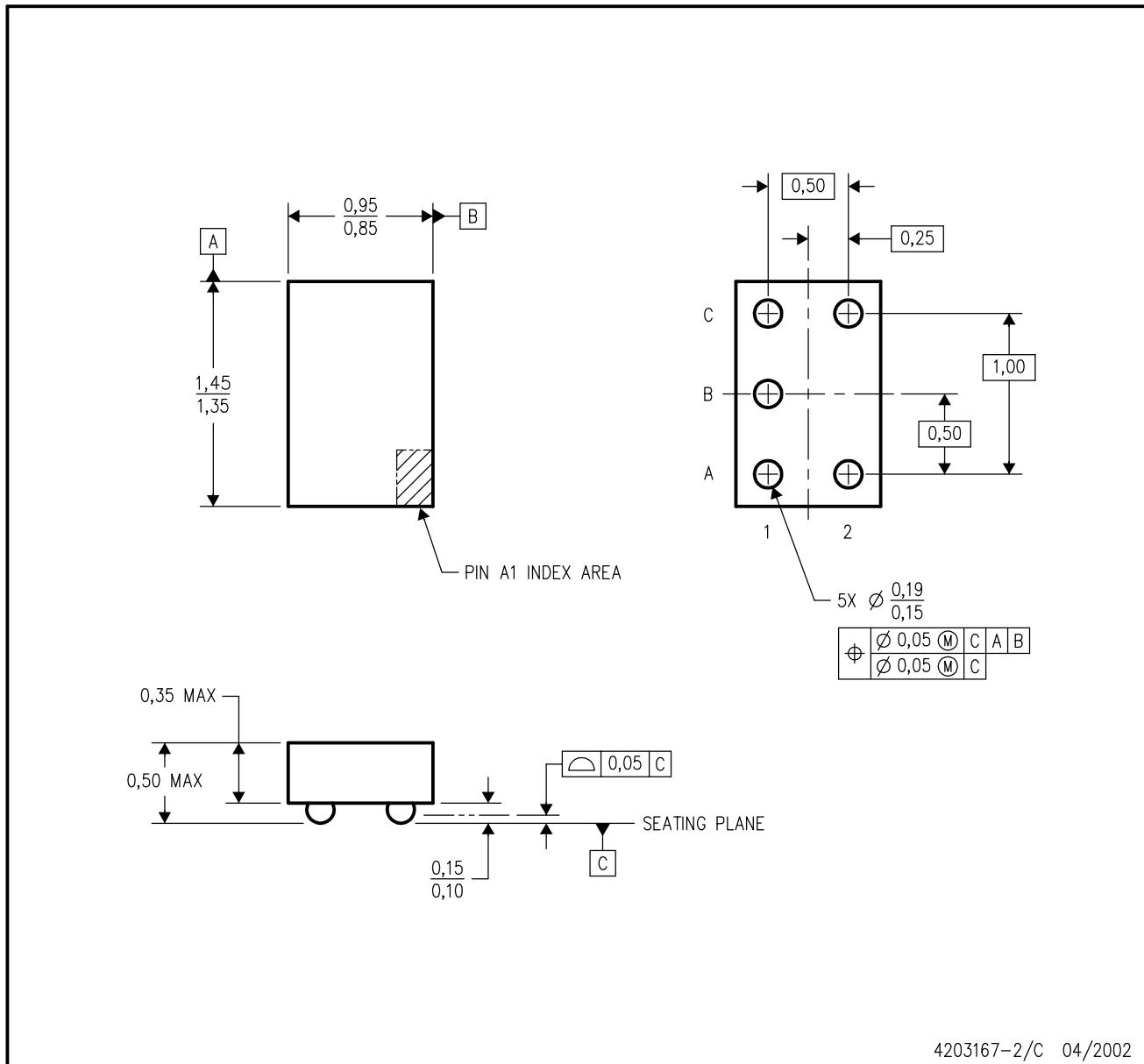


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. JEDEC package registration is pending.

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



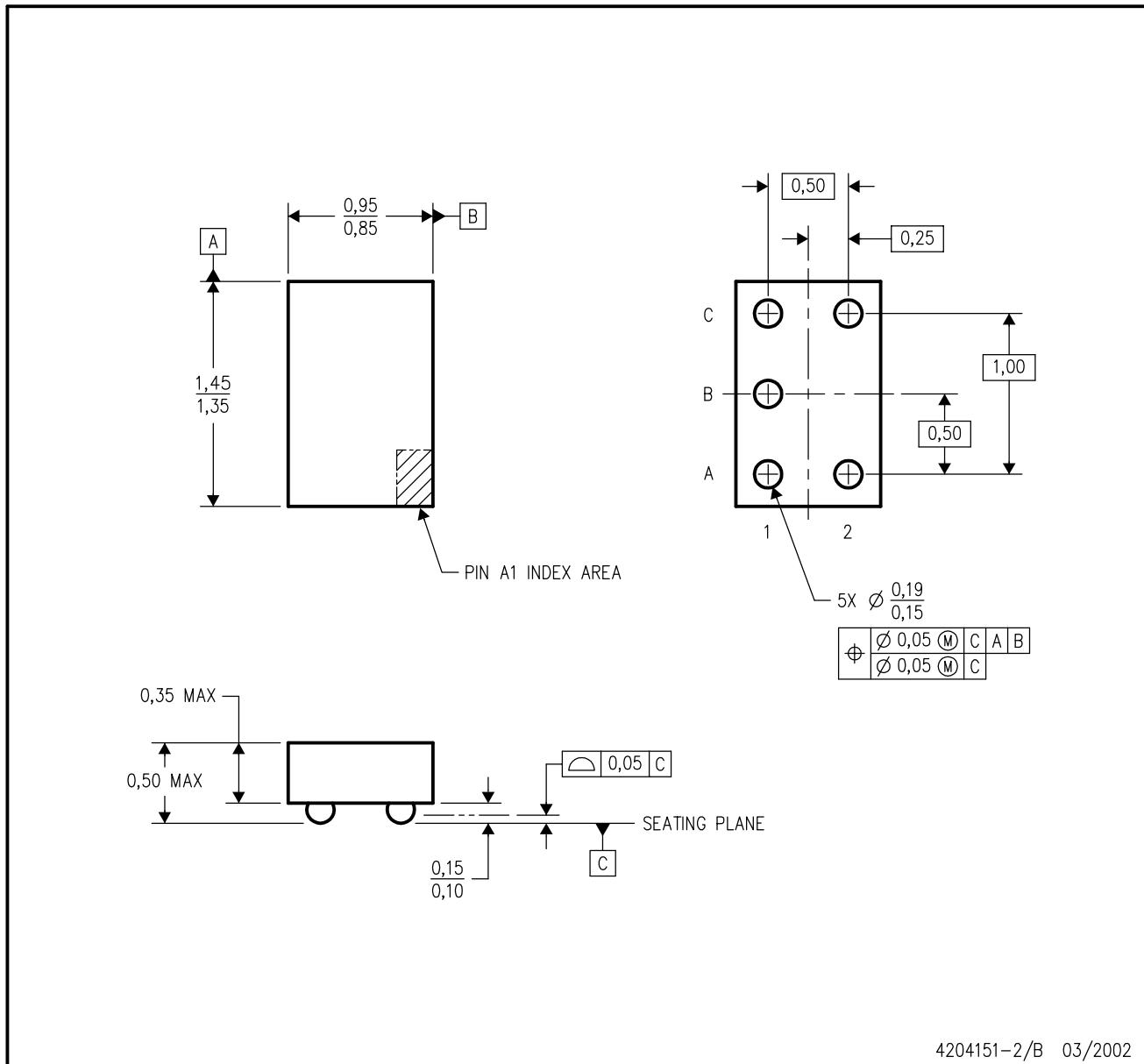
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- NanoStar™ package configuration.
- Package complies to JEDEC MO-211 variation EA.
- This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204151-2/B 03/2002

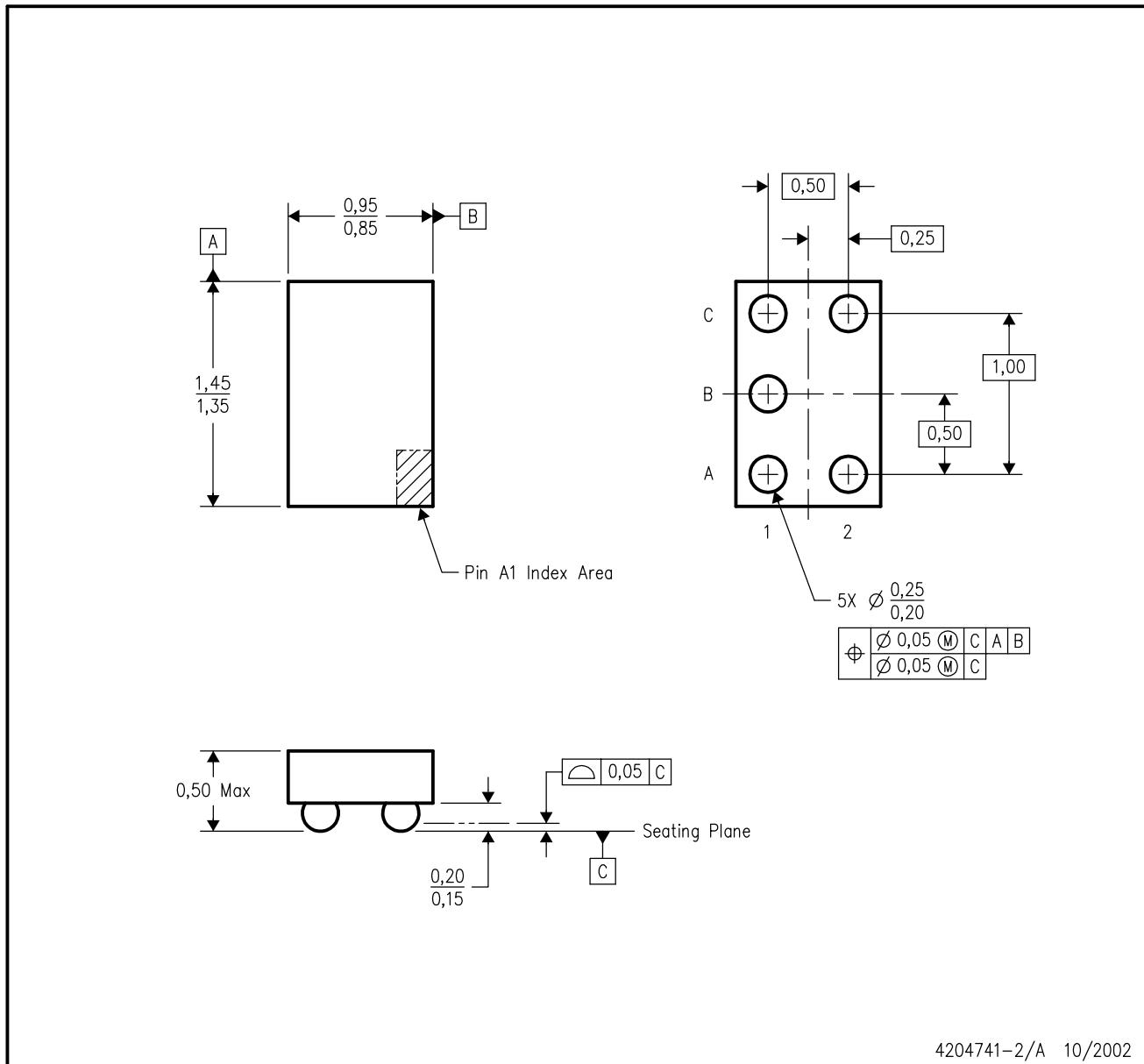
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- NanoFree™ package configuration.
- Package complies to JEDEC MO-211 variation EA.
- This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204741-2/A 10/2002

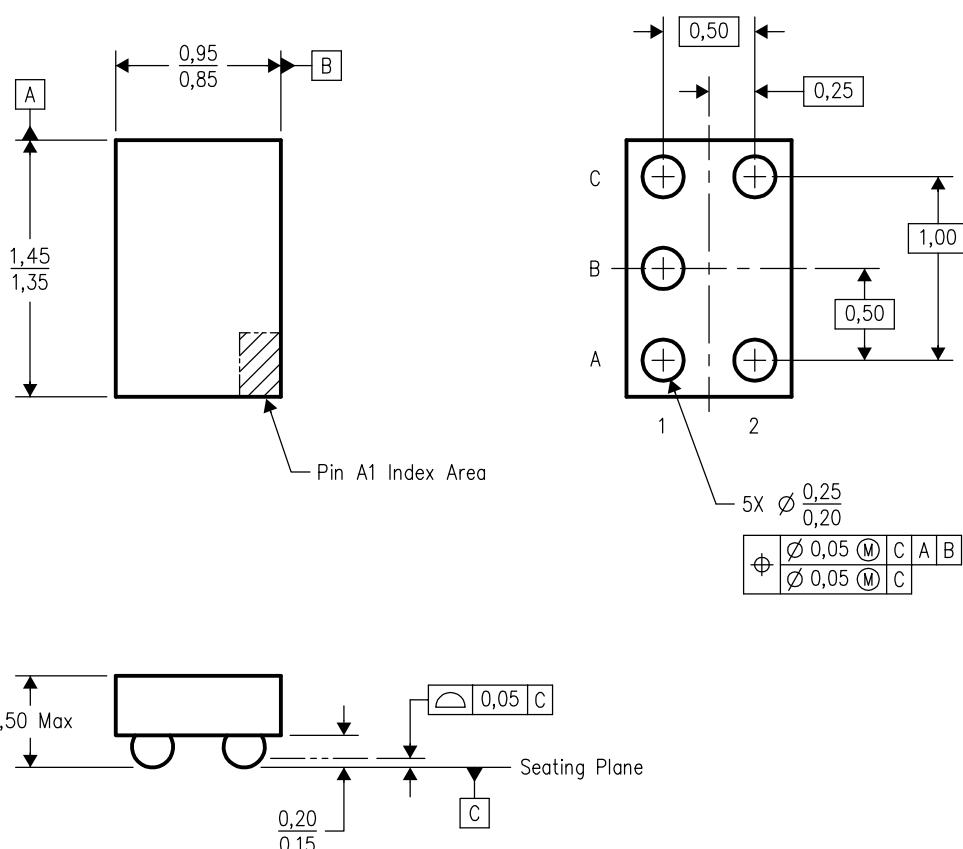
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- NanoFree™ package configuration.
- This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

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