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SN74LVC1G123
SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR
WITH SCHMITT-TRIGGER INPUTS
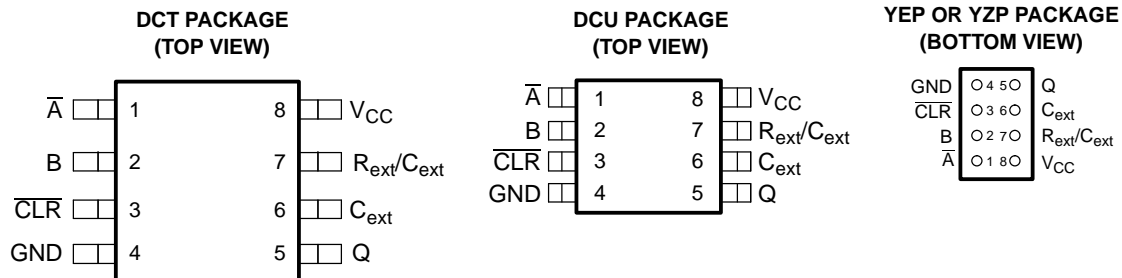SCES586A–JULY 2004–REVISED JUNE 2005

FEATURES

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Supports 5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 8 ns at 3.3 V**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **Schmitt-Trigger Circuitry on $\overline{A}$ and B Inputs for Slow Input Transition Rates**
- **Edge Triggered From Active-High or Active-Low Gated Logic Inputs**

- **Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

DCT PACKAGE
(TOP VIEW)

$\overline{A}$	1	8 V_{CC}
B	2	7 R_{ext}/C_{ext}
$\overline{CLR}$	3	6 C_{ext}
GND	4	5 Q

DCU PACKAGE
(TOP VIEW)

$\overline{A}$	1	8 V_{CC}
B	2	7 R_{ext}/C_{ext}
$\overline{CLR}$	3	6 C_{ext}
GND	4	5 Q

YEP OR YZP PACKAGE
(BOTTOM VIEW)

GND	4 5	Q
$\overline{CLR}$	3 6	C_{ext}
B	2 7	R_{ext}/C_{ext}
$\overline{A}$	1 8	V_{CC}

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74LVC1G123 is a single retriggerable monostable multivibrator designed for 1.65-V to 5.5-V V_{CC} operation.

This monostable multivibrator features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[2]
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74LVC1G123YEPR	_ _ _ D8_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G123YZPR	
	SSOP – DCT	Reel of 3000	SN74LVC1G123DCTR	C23_
		Reel of 250	SN74LVC1G123DCTT	
	VSSOP – DCU	Reel of 3000	SN74LVC1G123DCUR	C23_
		Reel of 250	SN74LVC1G123DCUT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
    DCU: The actual top-side marking has one additional character that designates the assembly/test site.
    YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DECSCRIPTION/ORDERING INFORMATION (CONTINUED)

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$ and B inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. $\overline{CLR}$ can be used to override $\overline{A}$ or B inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.
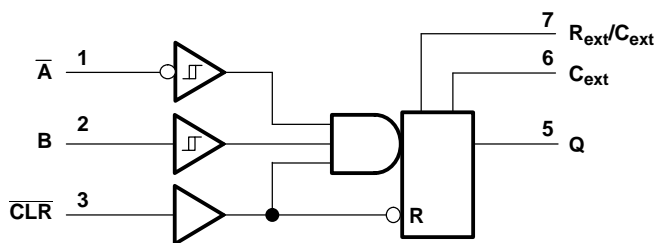
NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.
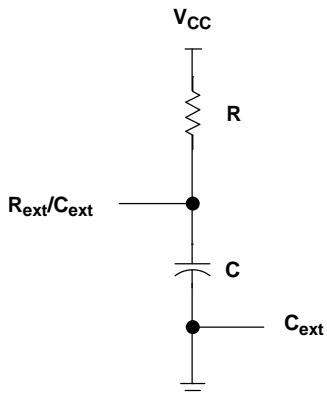
FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L[1]
X	X	L	L[1]
H	L	↑	⊓
H	↓	H	⊓
↑	L	H	⊓

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.
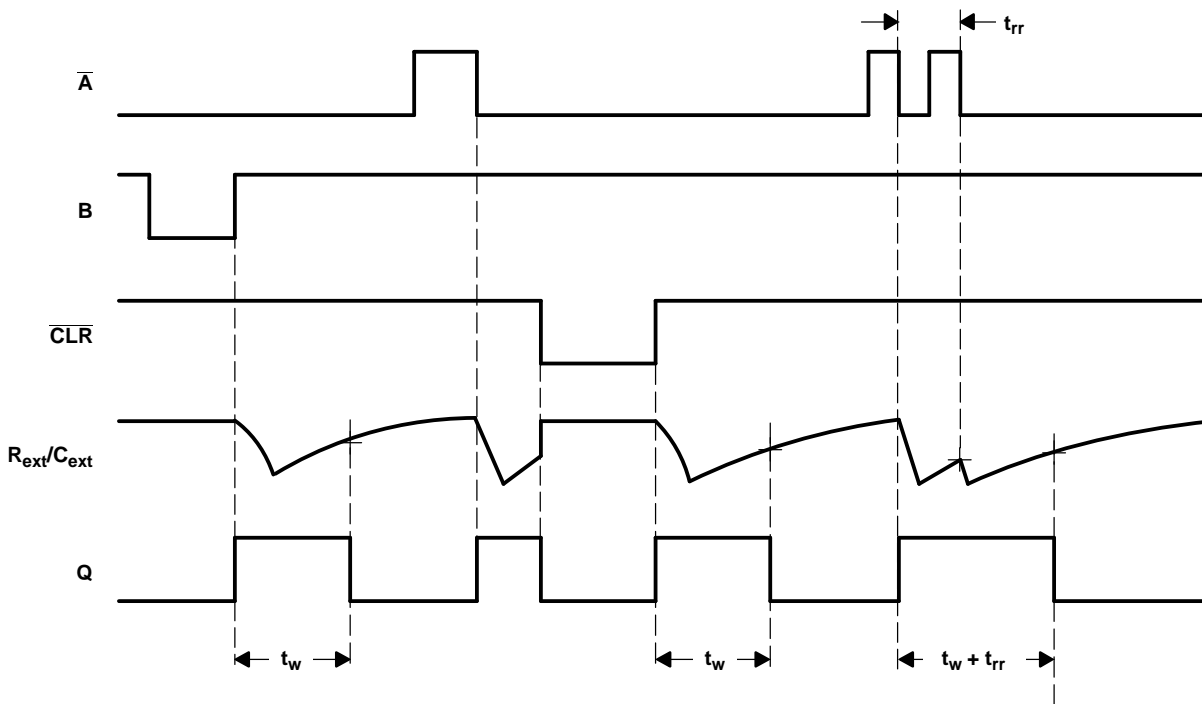
LOGIC DIAGRAM (POSITIVE LOGIC)

REQUIRED TIMING CIRCUIT

INPUT/OUTPUT TIMING DIAGRAM

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Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DCT package		220	°C/W
		DCU package		227	
		YEP/YZP package		102	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 3 V		−16	
				−24	
		V_{CC} = 4.5 V		−32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
R_{ext}[2]	External timing resistance	V_{CC} = 2 V	5 k		Ω
		V_{CC} ≥ 3 V	1 k		
T_A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) R_{ext}/C_{ext} is an I/O and must not be connected directly to GND or V_{CC}.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$		1.65 V to 5.5 V	$V_{CC} - 0.1$			V
		$I_{OH} = -4\ mA$		1.65 V		1.2		
		$I_{OH} = -8\ mA$		2.3 V		1.9		
		$I_{OH} = -16\ mA$		3 V		2.4		
		$I_{OH} = -24\ mA$				2.3		
		$I_{OH} = -32\ mA$		4.5 V		3.8		
V_{OL}		$I_{OL} = 100\ \mu A$		1.65 V to 5.5 V			0.1	V
		$I_{OL} = 4\ mA$		1.65 V			0.45	
		$I_{OL} = 8\ mA$		2.3 V			0.3	
		$I_{OL} = 16\ mA$		3 V			0.4	
		$I_{OL} = 24\ mA$					0.55	
		$I_{OL} = 32\ mA$		4.5 V			0.55	
I_I	R_{ext}/C_{ext}[2]	B = GND,	$\overline{A} = \overline{CLR} = V_{CC}$	1.65 V to 5.5 V			±0.25	μA
	$\overline{A}$, B, $\overline{CLR}$	$V_I = 5.5\ V$ or GND					±1	
I_{off}	$\overline{A}$, B, Q, $\overline{CLR}$	V_I or $V_O = 5.5\ V$		0			±10	μA
I_{CC}	Quiescent	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			20	μA
I_{CC}	Active state	$V_I = V_{CC}$ or GND,	$R_{ext}/C_{ext} = 0.5\ V_{CC}$	1.65 V			165	μA
				2.3 V			220	
				3 V			280	
				4.5 V			650	
				5.5 V			975	
C_i		$V_I = V_{CC}$ or GND		3.3 V		3		pF

(1) All typical values are at $V_{CC} = 3.3\ V$, $T_A = 25°C$.
(2) This test is performed with the terminal in the off-state condition.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			TEST CONDITIONS		$V_{CC} = 1.8\ V$ $\pm 0.15\ V$		$V_{CC} = 2.5\ V$ $\pm 0.2\ V$		$V_{CC} = 3.3\ V$ $\pm 0.3\ V$		$V_{CC} = 5\ V$ $\pm 0.5\ V$		UNIT
					MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
t_wIN	Pulse duration	$\overline{CLR}$			8		4		3		2.5		ns
		$\overline{A}$ or B trigger			8		4		3		2.5		
t_{rr}	Pulse retrigger time		$R_{ext} = 1\ k\Omega$	$C_{ext} = 100\ pF$						5.5		4.5	ns
				$C_{ext} = 100\ \mu F$						1.4		1.1	μs
			$R_{ext} = 5\ k\Omega$	$C_{ext} = 100\ pF$	75		45						ns
				$C_{ext} = 100\ \mu F$	1.8		1.4						μs

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15\ pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\ V$ $\pm 0.15\ V$			$V_{CC} = 2.5\ V$ $\pm 0.2\ V$		$V_{CC} = 3.3\ V$ $\pm 0.3\ V$		$V_{CC} = 5\ V$ $\pm 0.5\ V$		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q	7	18.5	52	4	17	3	11.5	2	7.6	ns
	$\overline{CLR}$		5	12.4	34	3	11.5	2	8	1.5	5.5	
	$\overline{CLR}$ trigger		7	17.4	54	4	15.5	3	10.5	2	7	

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Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q		6	18.6	57	3	18.5	2	12.5	1.5	8.2	ns
	$\overline{CLR}$			4	11.6	36.5	2	12.5	1.5	8.6	1.5	6	
	$\overline{CLR}$ trigger			5	17.3	59	2.5	17	2	11.5	1.5	7.5	
t_wOUT(2)		Q	C_{ext} = 28 pF, R_{ext} = 2 kΩ		225	600	190	220	170	200	150	180	ns
			C_{ext} = 0.01 μF, R_{ext} = 10 kΩ		100	110	100	110	100	110	100	110	μs
			C_{ext} = 0.1 μF, R_{ext} = 10 kΩ		1	1.1	1	1.1	1	1.1	1	1.1	ms

(1) T_A = 25°C
(2) t_w = Duration of pulse at Q output

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
				TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$\overline{A}$ = low, B = high, $\overline{CLR}$ = 10 MHz	R_{ext} = 1 kΩ, No C_{ext}			35	37	pF
			R_{ext} = 5 kΩ, No C_{ext}	41	40			

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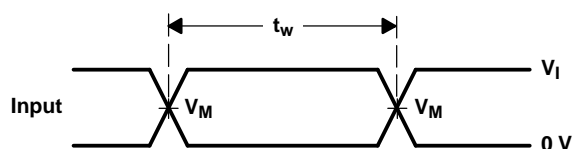**TEXAS INSTRUMENTS**
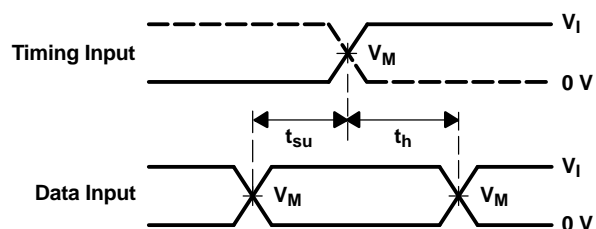www.ti.com

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V $\pm$ 0.15 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
3.3 V $\pm$ 0.3 V	3 V	$\leq$2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V $\pm$ 0.5 V	V_{CC}	$\leq$2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
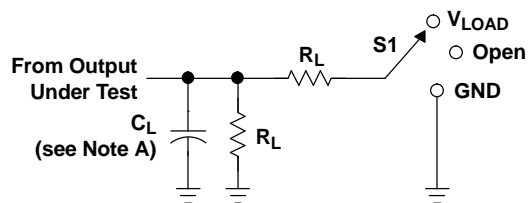**INVERTING AND NONINVERTING OUTPUTS**

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.
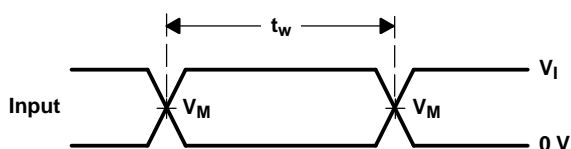
Figure 1. Load Circuit and Voltage Waveforms

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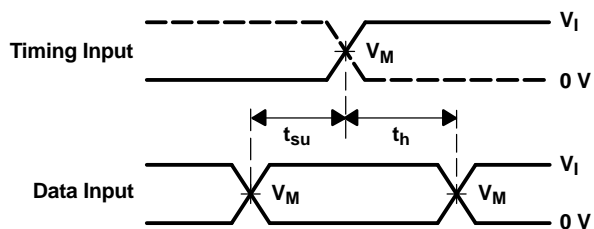
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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

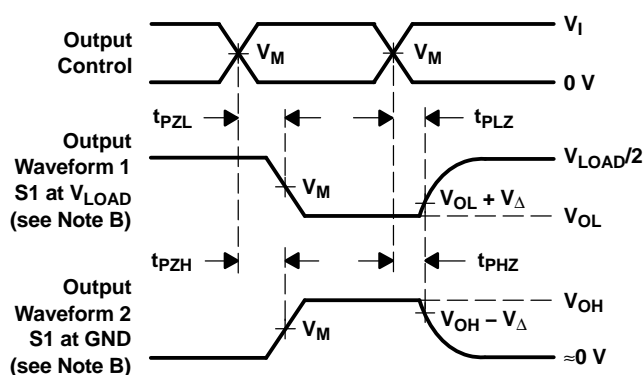| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
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Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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APPLICATION INFORMATION[1]

OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE

Figure 3.

OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE

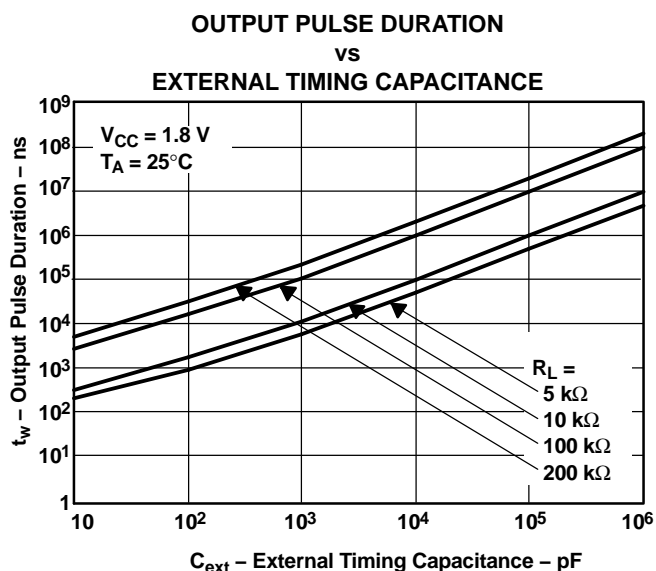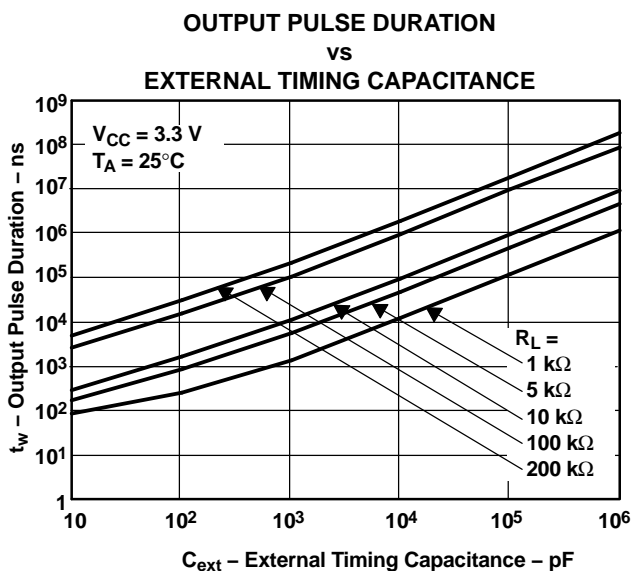**Figure 4.**

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.
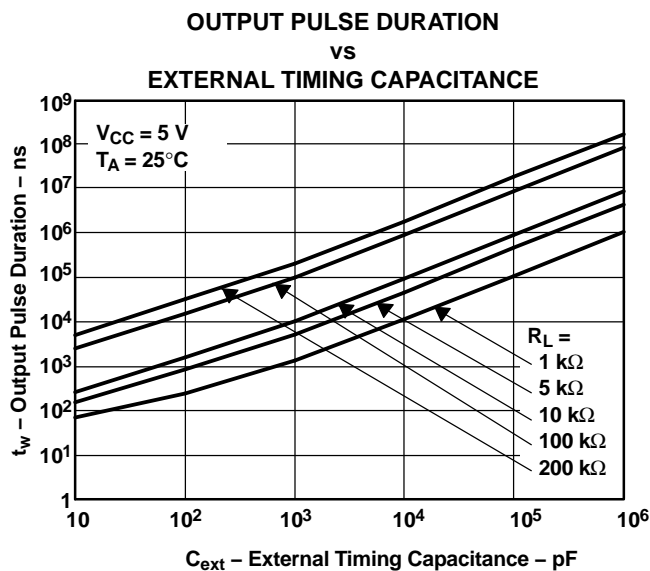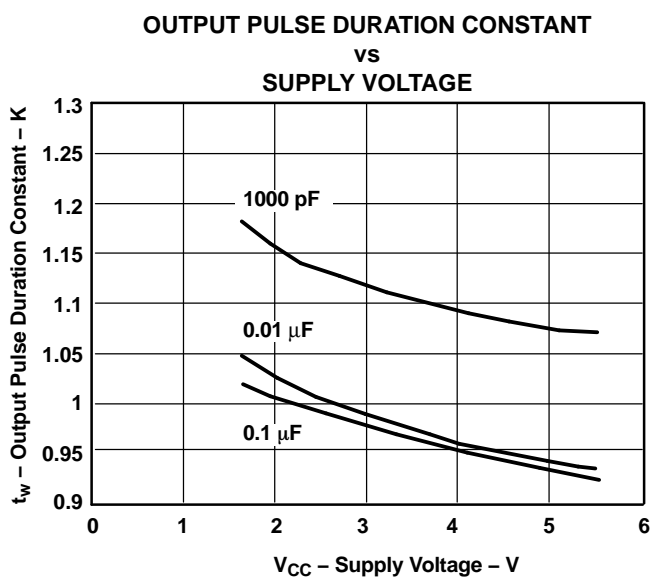
OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE

Figure 5.

OUTPUT PULSE DURATION CONSTANT
vs
SUPPLY VOLTAGE

Figure 6.

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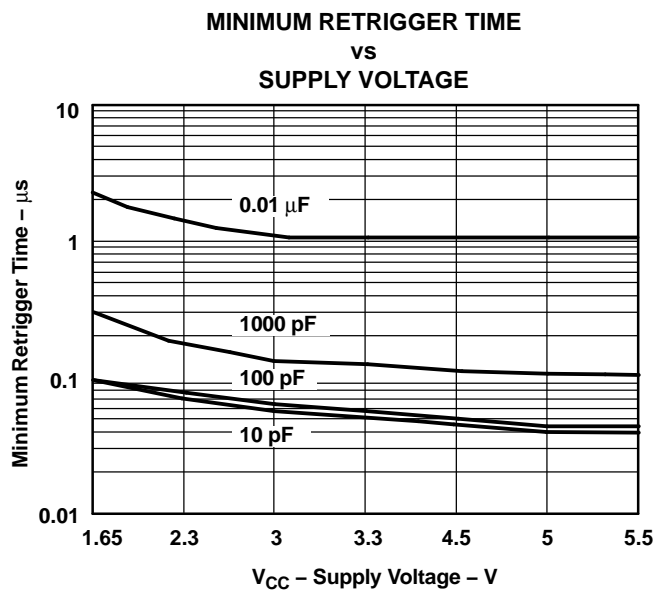**TEXAS INSTRUMENTS**
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**MINIMUM RETRIGGER TIME
vs
SUPPLY VOLTAGE**

Figure 7.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74LVC1G123DCTRE4	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCTTE4	ACTIVE	SM8	DCT	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCTR	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCTT	ACTIVE	SM8	DCT	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123YEPR	NRND	WCSP	YEP	8	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G123YZPR	ACTIVE	WCSP	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
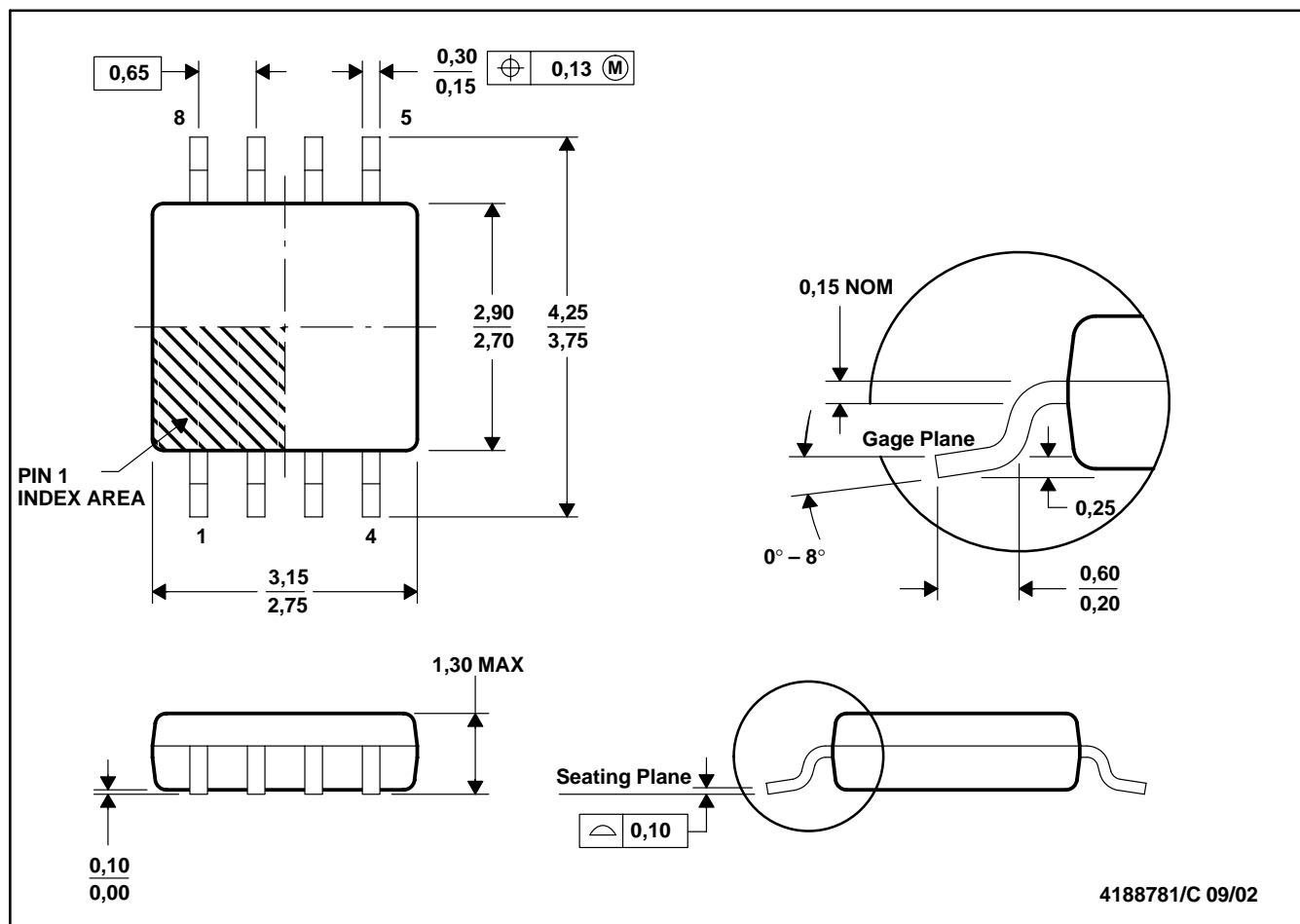
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCT (R-PDSO-G8)   **PLASTIC SMALL-OUTLINE PACKAGE**

4188781/C 09/02

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion
  D. Falls within JEDEC MO-187 variation DA.

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DCU (R−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE (DIE DOWN)

4200503/F 07/05
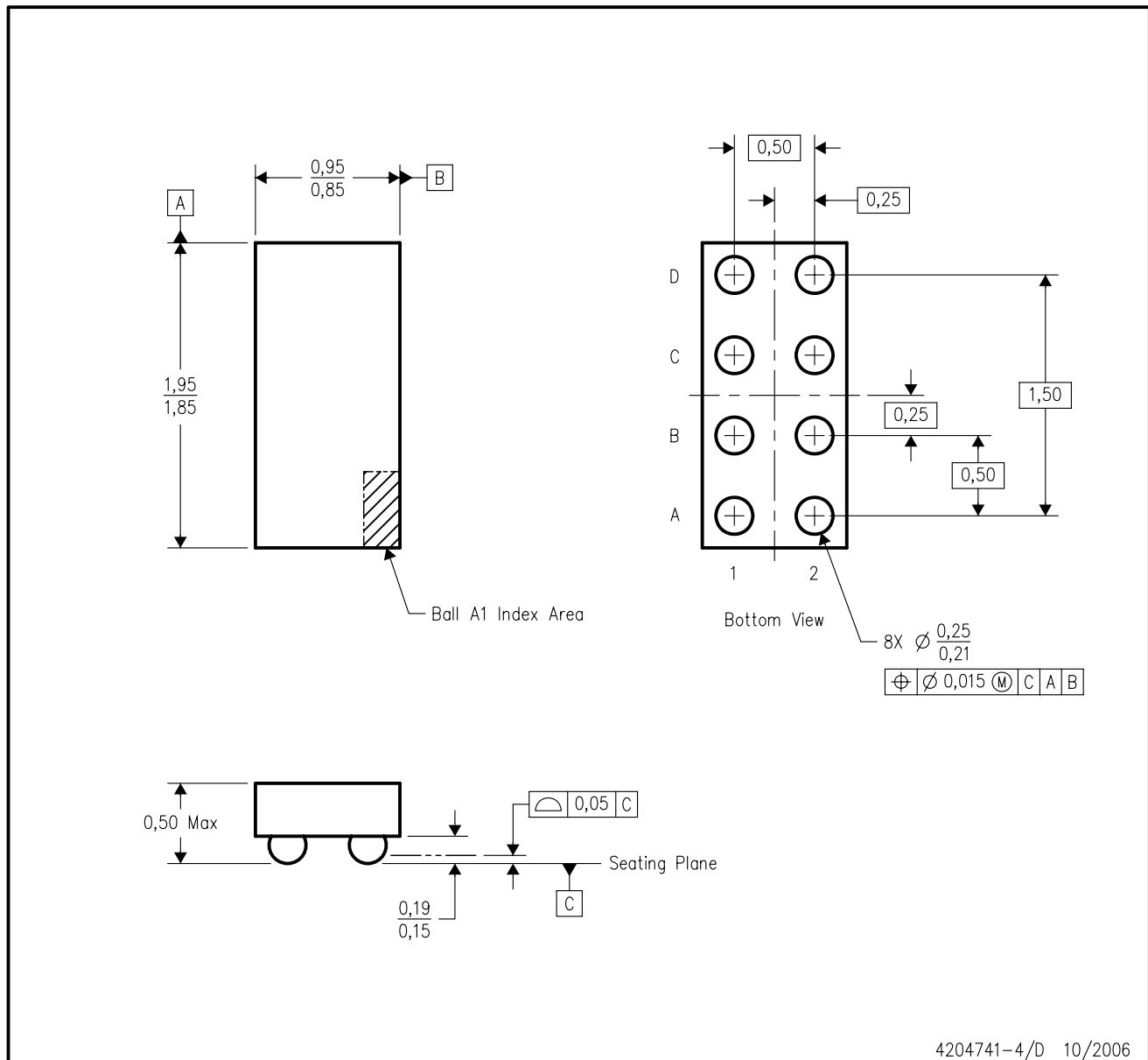
NOTES: A.   All linear dimensions are in millimeters.
           B.   This drawing is subject to change without notice.
           C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
           D.   Falls within JEDEC MO−187 variation CA.

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YZP (R−XBGA−N8)   DIE−SIZE BALL GRID ARRAY

0,95
0,85

B

A

1,95
1,85

Ball A1 Index Area

0,50

0,25

D

C

B

A

1   2

Bottom View

0,25

1,50

0,50

8X Ø 0,25
       0,21

⊕ Ø 0,015 Ⓜ C A B

0,50 Max

0,19
0,15

Seating Plane

0,05 C

C

4204741−4/D 10/2006
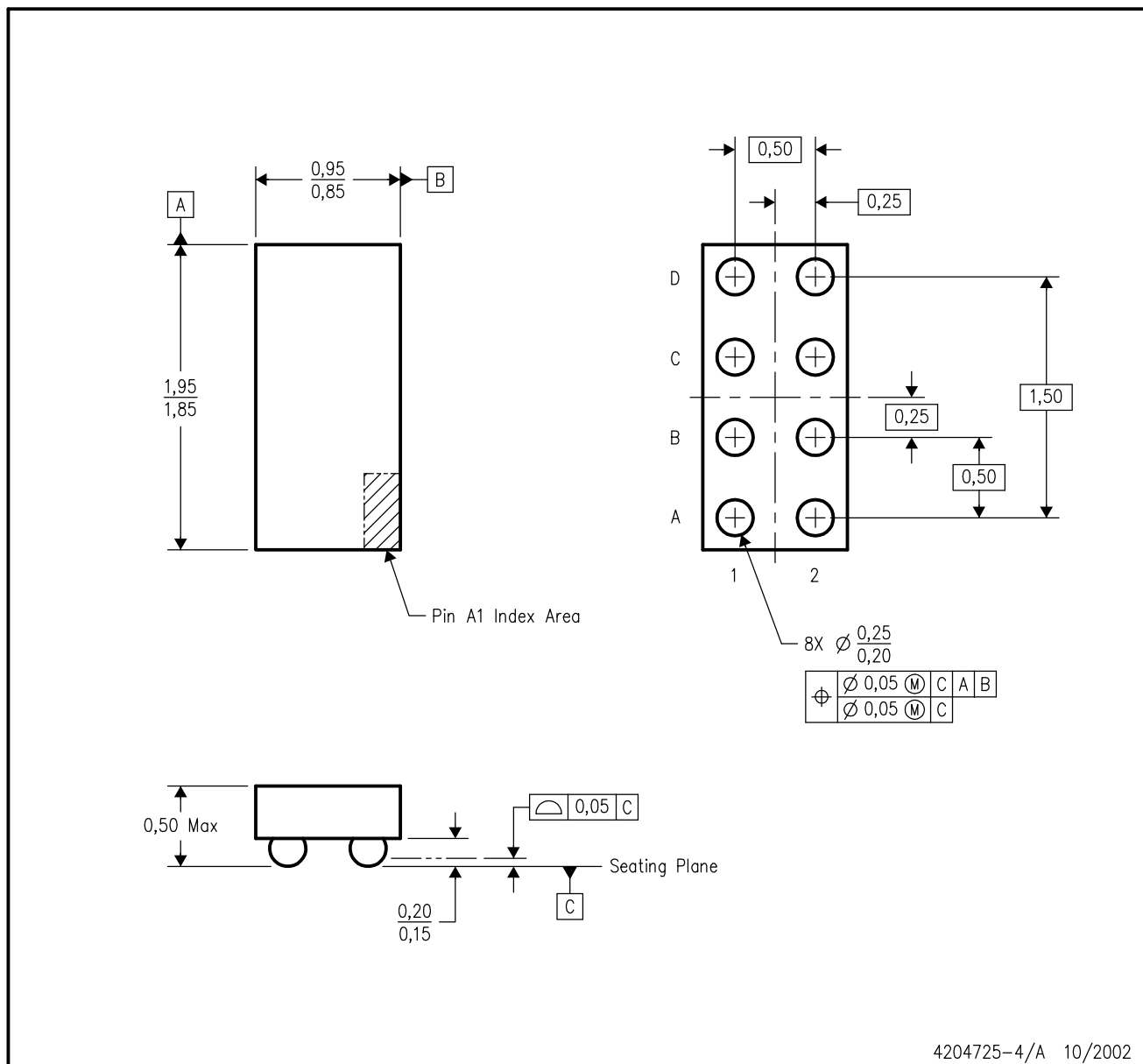
NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   NanoFree™ package configuration.
         D.   This package is lead−free.   Refer to the 8 YEP package (drawing 4204725) for tin−lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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YEP (R−XBGA−N8)   DIE−SIZE BALL GRID ARRAY

0,95
0,85

A   B

1,95
1,85

Pin A1 Index Area

0,50

0,25

D   C   B   A

1   2

1,50

0,25

0,50

8X ∅ 0,25
        0,20

⊕ | ∅ 0,05 (M) | C | A | B
   | ∅ 0,05 (M) | C

0,50 Max

0,05 C

Seating Plane

0,20
0,15

C

4204725−4/A   10/2002

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   NanoStar™ package configuration.
         D.   This package is tin−lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead−free.

NanoStar is a trademark of Texas Instruments.

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