

**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIN9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

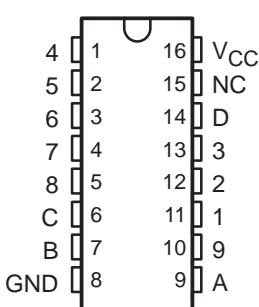
'147, 'LS147

- Encode 10-Line Decimal to 4-Line BCD
- Applications Include:
 - Keyboard Encoding
 - Range Selection

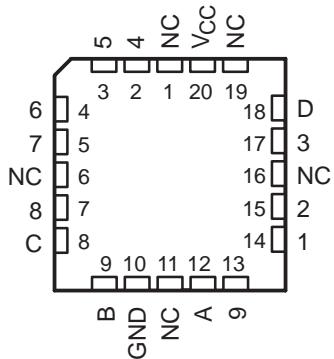
SN54147, SN54LS147 . . . J OR W PACKAGE

SN74147, SN74LS147 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS147 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

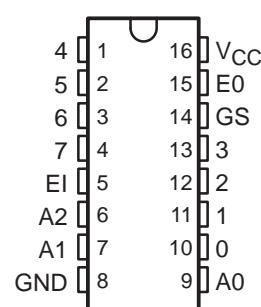
'148, 'LS148

- Encode 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
 - n-Bit Encoding
 - Code Converters and Generators

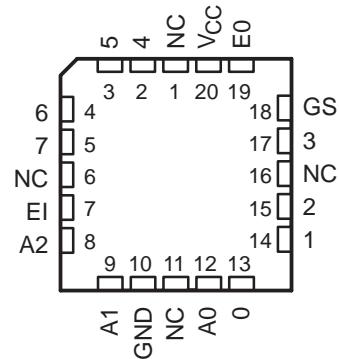
SN54148, SN54LS148 . . . J OR W PACKAGE

SN74148, SN74LS148 . . . D, N, OR NS PACKAGE

(TOP VIEW)



SN54LS148 . . . FK PACKAGE
(TOP VIEW)



NOTE: The SN54147, SN54LS147, SN54148, SN74147, SN74LS147, and SN74148 are obsolete and are no longer supplied.



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**SN54147, SN54148, SN54LS147, SN54LS148
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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description/ordering information

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 devices encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition, as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 devices encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54/74LS load, respectively.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS148N	SN74LS148N
	SOIC – D	Tube	SN74LS148D	LS148
		Tape and reel	SN74LS148DR	
-55°C to 125°C	SOP – NS	Tape and reel	SN74LS148NSR	74LS148
	CDIP – J	Tube	SNJ54LS148J	SNJ54LS148J
	CFP – W	Tube	SNJ54LS148W	SNJ54LS148W
	LCCC – FK	Tube	SNJ54LS148FK	SNJ54LS148FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE – '147, 'LS147

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (T1M9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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FUNCTION TABLE – '148, 'LS148

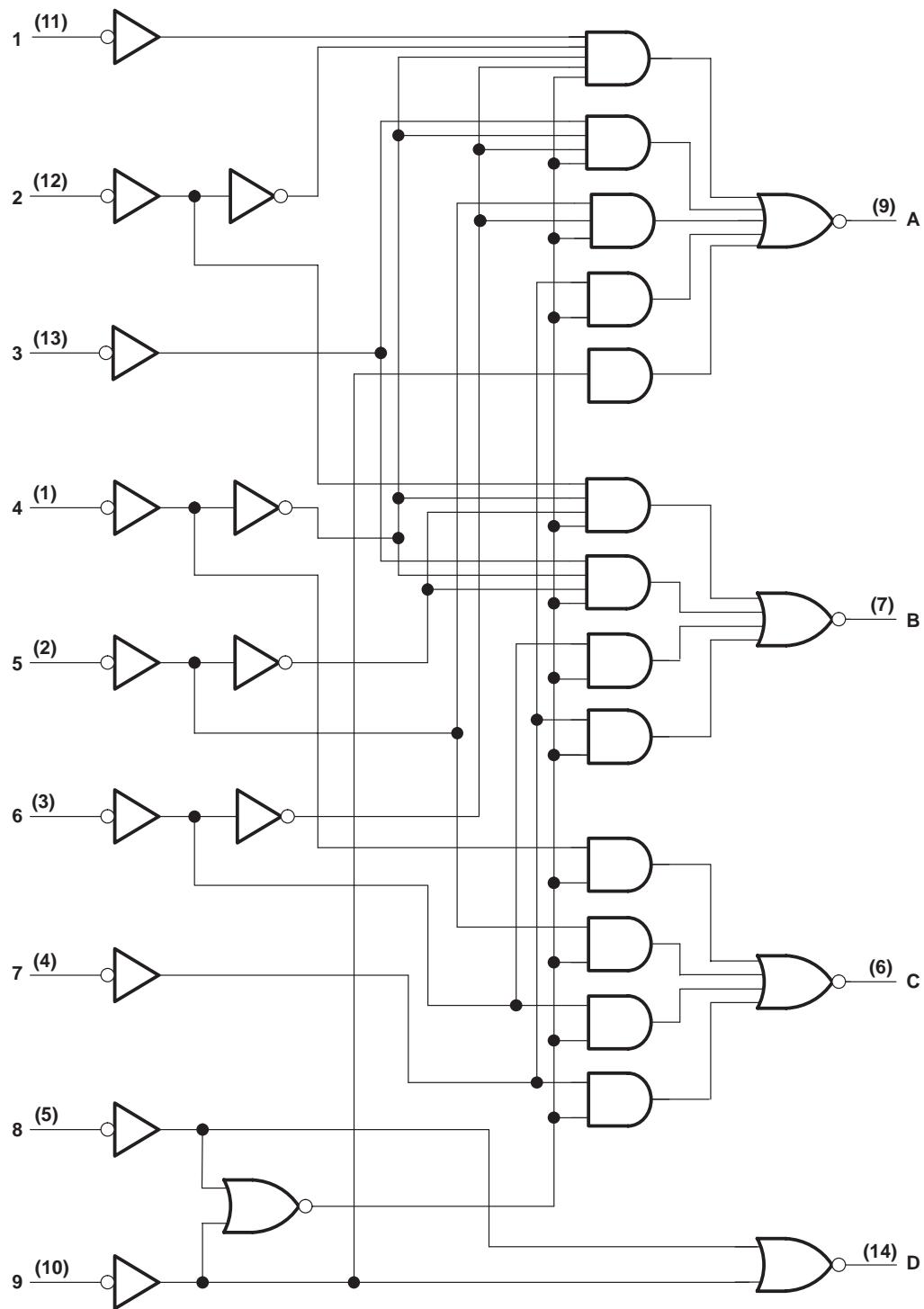
EI	INPUTS							OUTPUTS					
	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant

**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (T1M9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

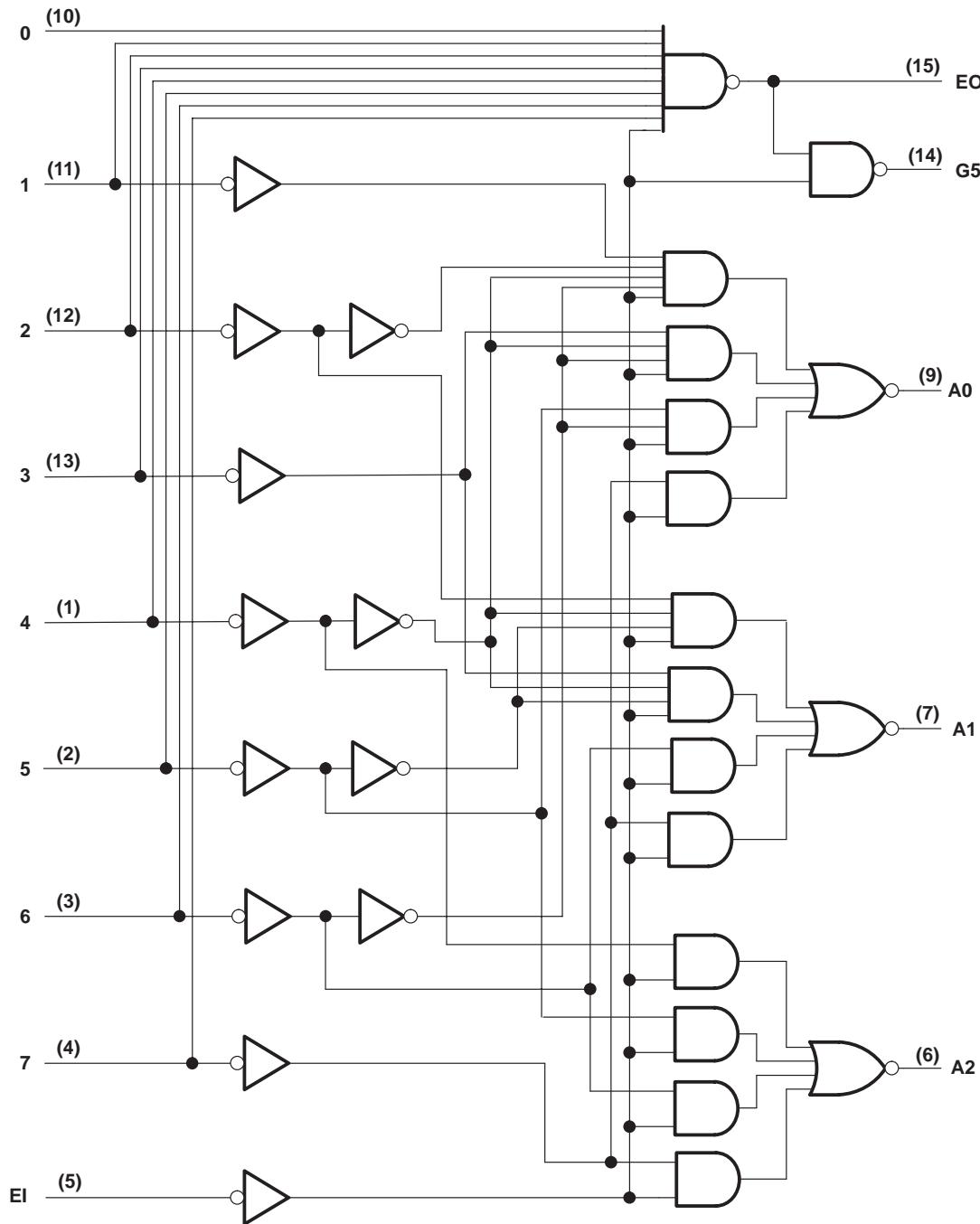
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'147, 'LS147 logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

'148, 'LS148 logic diagram (positive logic)



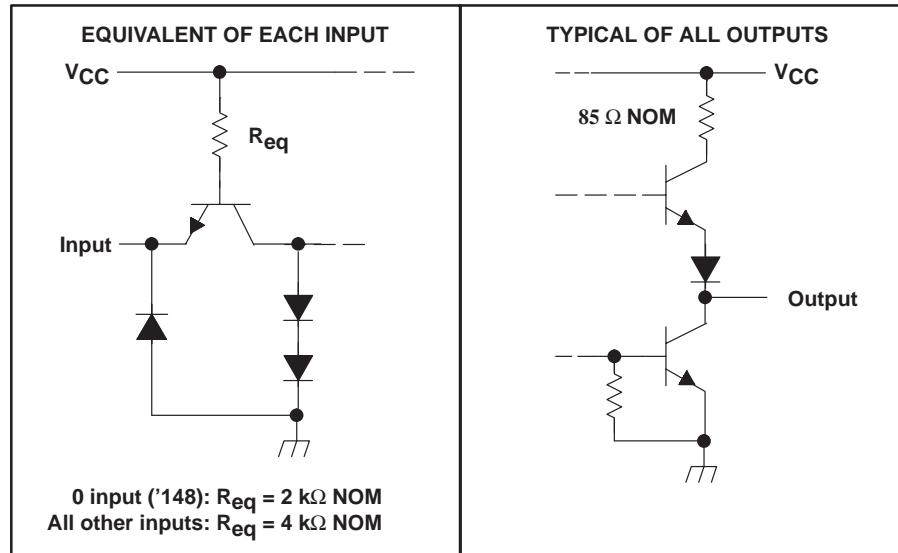
Pin numbers shown are for D, J, N, NS, and W packages.

**SN54147, SN54148, SN54LS147, SN54LS148
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

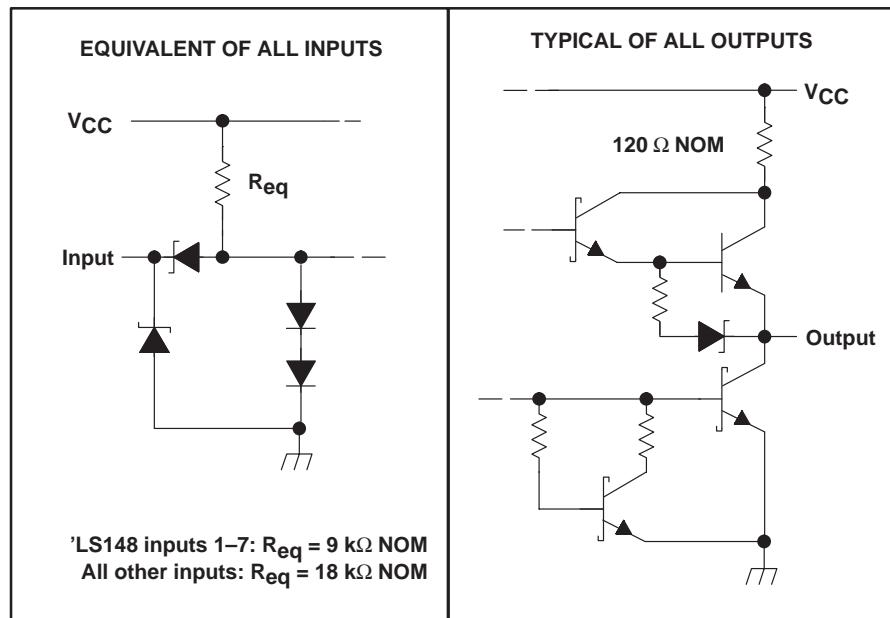
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schematics of inputs and outputs

'147, '148



'LS147, 'LS148



SN54147, SN54148, SN54LS147, SN54LS148 SN74147, SN74148 (TMS148), SN74LS147, SN74LS148 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I : '147, '148	5.5 V
'LS147, 'LS148	7 V
Inter-emitter voltage: '148 only (see Note 2)	5.5 V
Package thermal impedance θ_{JA} (see Note 3): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Storage temperature range, T_{STG}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values, except inter-emitter voltage, are with respect to the network ground terminal.

1. Voltage drops, input-output currents, voltage, and current respect to the network ground connection.
2. This is the voltage between two emitters of a multiple-emitter transistor. For '148 circuits, this rating applies between any two of the eight data lines, 0 through 7.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		SN54'			SN74'			SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-800			-800			-400			-400	µA
I _{OL}	Low-level output current			16			16			4			8	mA
T _A	Operating free-air temperature	-55	125	0	70	-55	125	0	70	0	70	0	70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54147, SN54148, SN54LS147, SN54LS148
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	'147			'148			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage		2		2				V
V _{IL}	Low-level input voltage			0.8			0.8		V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA		-1.5			-1.5		V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -800 μ A	2.4	3.3		2.4	3.3		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	Input current at maximum input voltage	V _{CC} = MIN, V _I = 5.5 V		1			1		mA
I _{IH}	High-level input current	0 input	V _{CC} = MAX, V _I = 2.4 V					40	μ A
I _{IL}	Low-level input current	Any input except 0			40			80	
I _{OS}	Short-circuit output current [§]		V _{CC} = MAX	-35	-85	-35	-85		mA
I _{CC}	Supply current	V _{CC} = MAX (See Note 5)	Condition 1	50	70	40	60	mA	
			Condition 2	42	62	35	55		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time.

NOTE 5: For '147, I_{CC} (Condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open. For '148, I_{CC} (Condition 1) is measured with inputs 7 and E_I grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open.

SN54147, SN74147 switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _{PLH}	Any	Any	In-phase output	C _L = 15 pF, R _L = 400 Ω	9	14		ns	
t _{PHL}					7	11			
t _{PLH}		Any	Out-of-phase output		13	19		ns	
t _{PHL}					12	19			

**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (T1M9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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SN54148, SN74148 switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}	1–7	A0, A1, or A2	In-phase output	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	10	15		ns	
t_{PHL}					9	14			
t_{PLH}		A0, A1, or A2	Out-of-phase output		13	19		ns	
t_{PHL}					12	19			
t_{PLH}		0–7	EO		6	10		ns	
t_{PHL}					14	25			
t_{PLH}		0–7	GS		18	30		ns	
t_{PHL}					14	25			
t_{PLH}	EI	A0, A1, or A2	In-phase output		10	15		ns	
t_{PHL}					10	15			
t_{PLH}		GS	In-phase output		8	12		ns	
t_{PHL}					10	15			
t_{PLH}	EI	EO	In-phase output		10	15		ns	
t_{PHL}					17	30			

[†] t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS'			SN74LS'			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage		2		2				V
V_{IL}	Low-level input voltage			0.7		0.8			V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$,				-1.5		-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$,	$V_{IH} = 2 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ MAX}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4	V
			$I_{OL} = 8 \text{ mA}$				0.35	0.5	
I_I	Input current at maximum input voltage	'LS148 inputs 1–7	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.2		0.2		mA
		All other inputs			0.1		0.1		
I_{IH}	High-level input current	'LS148 inputs 1–7	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		40		40		μA
		All other inputs			20		20		
I_{IL}	Low-level input current	'LS148 inputs 1–7	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.8		-0.8		mA
		All other inputs			-0.4		-0.4		
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$		-20	-100	-20	-100		mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$ (See Note 6)	Condition 1	12	20	12	20		mA
			Condition 2	10	17	10	17		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 6: For 'LS147, I_{CC} (Condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open. For 'LS148, I_{CC} (Condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open.

**SN54147, SN54148, SN54LS147, SN54LS148
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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SN54LS147, SN74LS147 switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}	Any	Any	In-phase output	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$	12	18		ns	
t_{PHL}					12	18			
t_{PLH}		Any	Out-of-phase output		21	33		ns	
t_{PHL}					15	23			

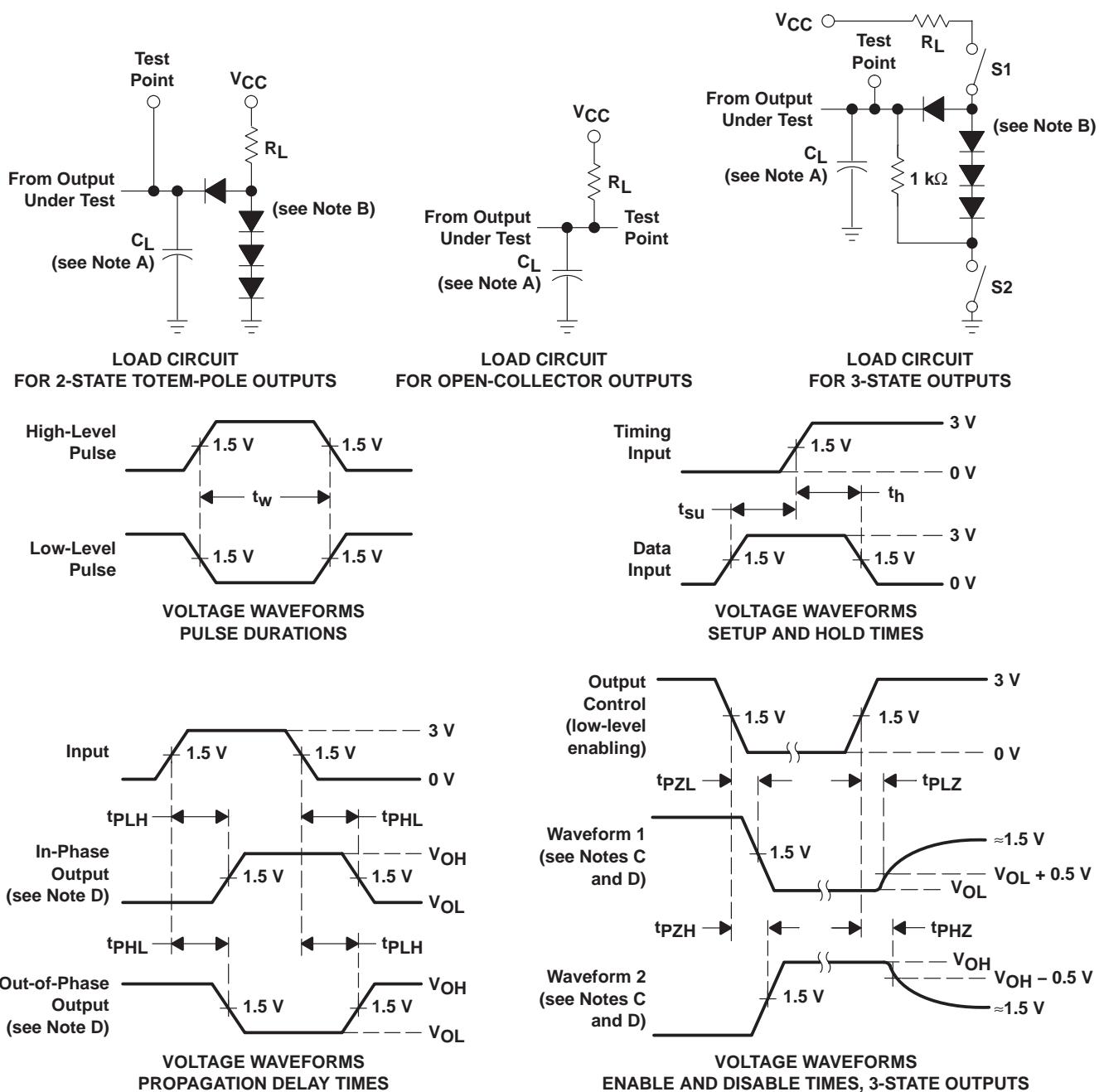
SN54LS148, SN74LS148 switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ (see Figure 2)

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}	1–7	A0, A1, or A2	In-phase output	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$	14	18		ns	
t_{PHL}					15	25			
t_{PLH}		A0, A1, or A2	Out-of-phase output		20	36		ns	
t_{PHL}					16	29			
t_{PLH}	0–7	EO	Out-of-phase output		7	18		ns	
t_{PHL}					25	40			
t_{PLH}		GS	In-phase output		35	55		ns	
t_{PHL}					9	21			
t_{PLH}	EI	A0, A1, or A2	In-phase output		16	25		ns	
t_{PHL}					12	25			
t_{PLH}		GS	In-phase output		12	17		ns	
t_{PHL}					14	36			
t_{PLH}	EI	EO	In-phase output		12	21		ns	
t_{PHL}					23	35			

[†] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION
 SERIES 54/74 DEVICES



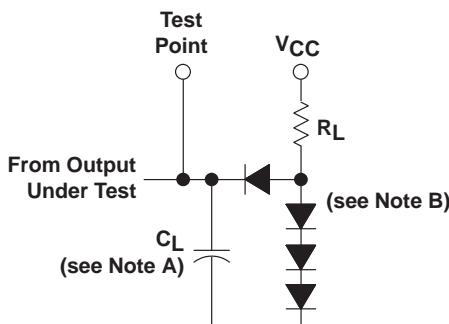
NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PZL} ; S1 is open, and S2 is closed for t_{PZH} ; S1 is closed, and S2 is open for t_{PLZ} .
 E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7 \text{ ns}$ for Series 54/74 devices and t_r and $t_f \leq 2.5 \text{ ns}$ for Series 54S/74S devices.
 F. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

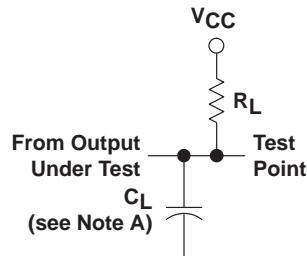
**SN54147, SN54148, SN54LS147, SN54LS148
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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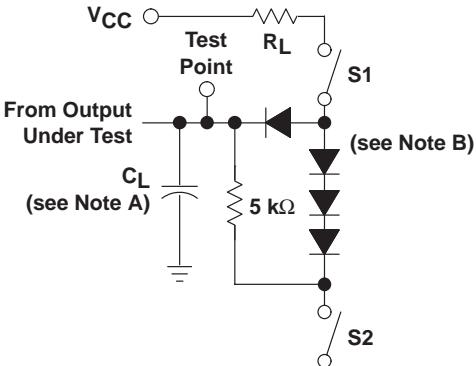
**PARAMETER MEASUREMENT INFORMATION
 SERIES 54LS/74LS DEVICES**



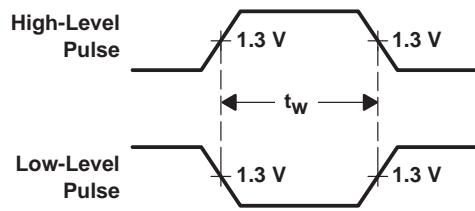
LOAD CIRCUIT
 FOR 2-STATE TOTEM-POLE OUTPUTS



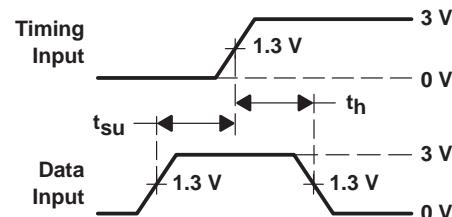
LOAD CIRCUIT
 FOR OPEN-COLLECTOR OUTPUTS



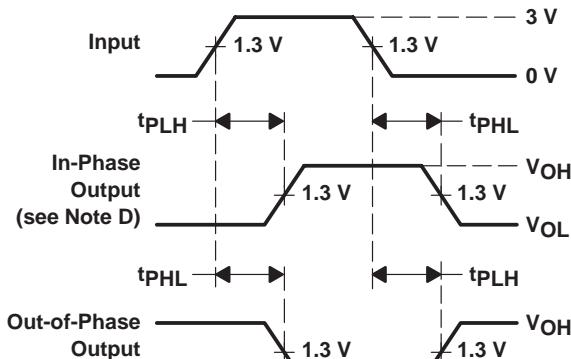
LOAD CIRCUIT
 FOR 3-STATE OUTPUTS



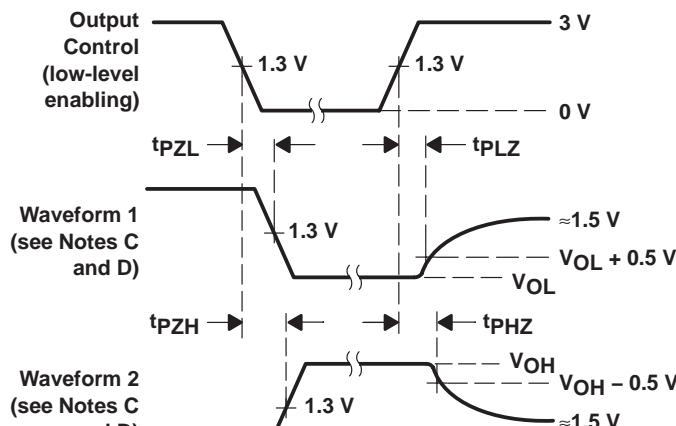
VOLTAGE WAVEFORMS
 PULSE DURATIONS



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:

- C_L includes probe and jig capacitance.
- All diodes are 1N3064 or equivalent.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PZL} ; S1 is open, and S2 is closed for t_{PZH} ; S1 is closed, and S2 is open for t_{PLZ} .
- Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O \approx 50 \Omega$, $t_r \leq 1.5 \text{ ns}$, $t_f \leq 2.6 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

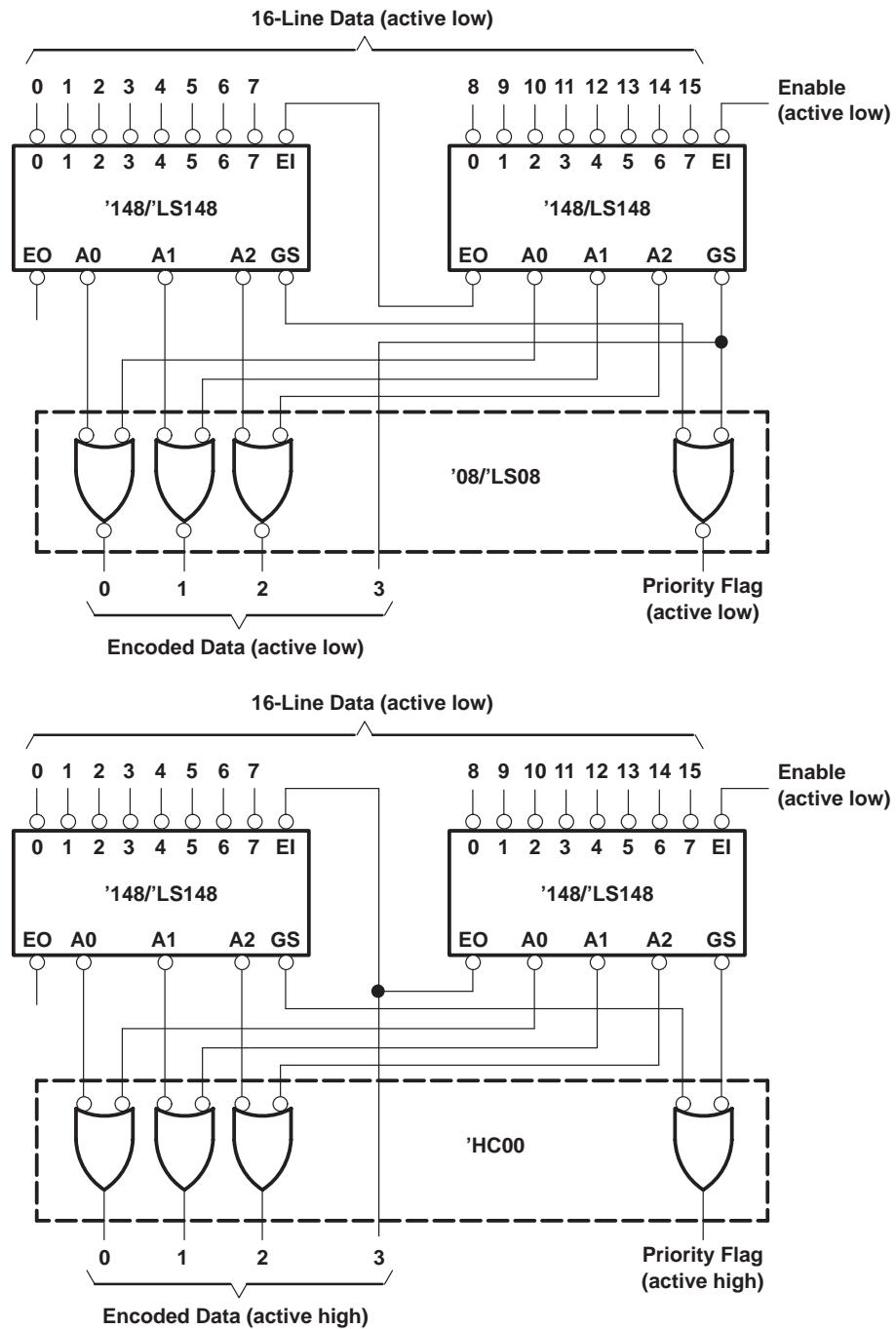


Figure 3. Priority Encoder for 16 Bits

Because the '147/LS147 and '148/LS148 devices are combinational logic circuits, wrong addresses can appear during input transients. Moreover, for the '148/LS148 devices, a change from high to low at EI can cause a transient low on GS when all inputs are high. This must be considered when strobing the outputs.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
78027012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
7802701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
7802701FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
JM38510/36001B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/36001BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
JM38510/36001BFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SN54148J	OBsolete	CDIP	J	16		TBD	Call TI	Call TI
SN54LS148J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN74147N	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN74148J	OBsolete	CDIP	J	16		TBD	Call TI	Call TI
SN74148N	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN74148N3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN74LS147DR	OBsolete	SOIC	D	16		TBD	Call TI	Call TI
SN74LS147N	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN74LS148D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LS148DE4	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LS148DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LS148DRE4	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LS148J	OBsolete	CDIP	J	16		TBD	Call TI	Call TI
SN74LS148N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS148N3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN74LS148NSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LS148NSRE4	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SNJ54148J	OBsolete	CDIP	J	16		TBD	Call TI	Call TI
SNJ54148W	OBsolete	CFP	W	16		TBD	Call TI	Call TI
SNJ54LS148FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS148J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS148W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

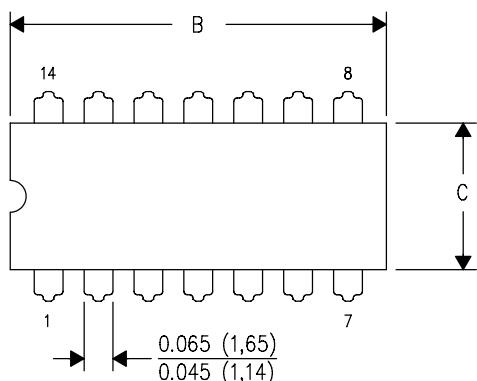
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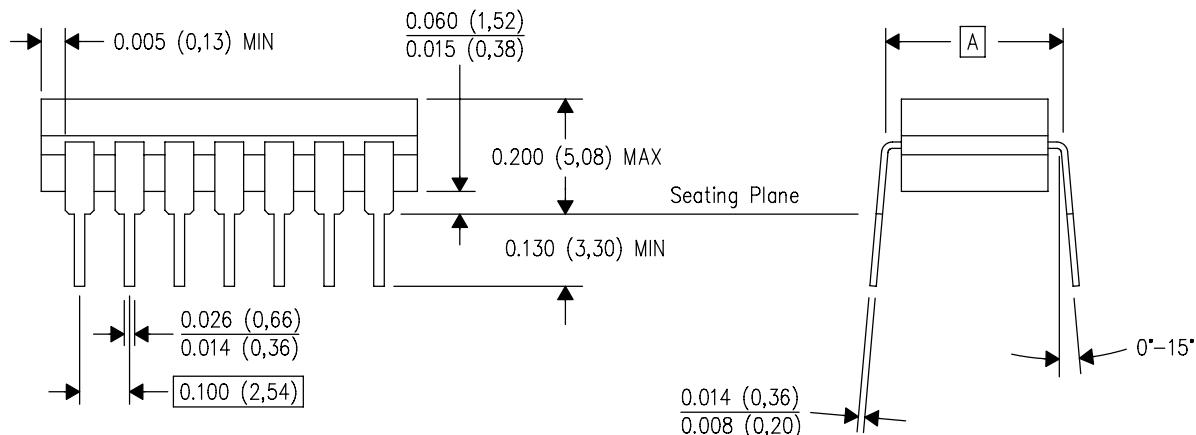
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

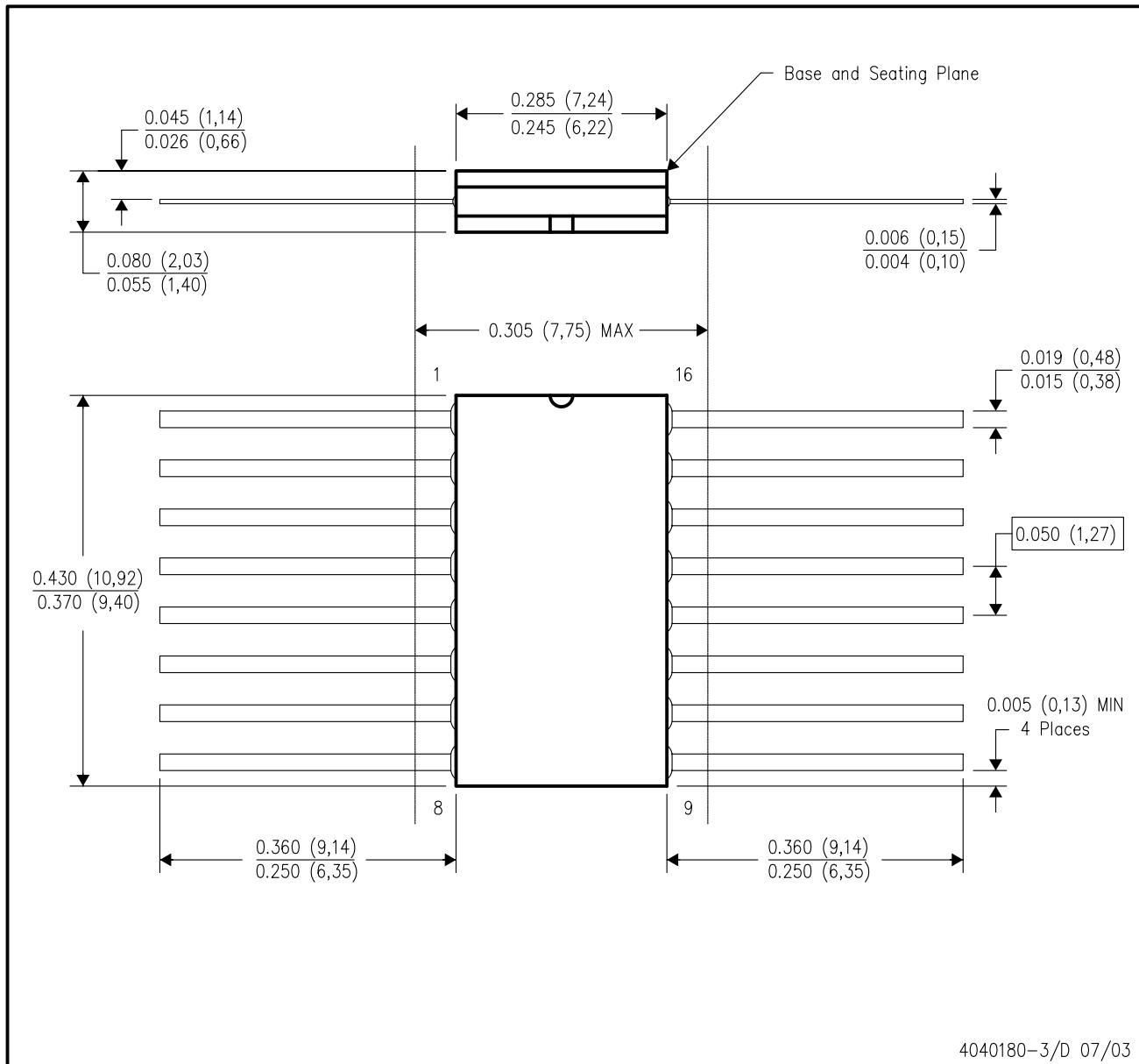


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



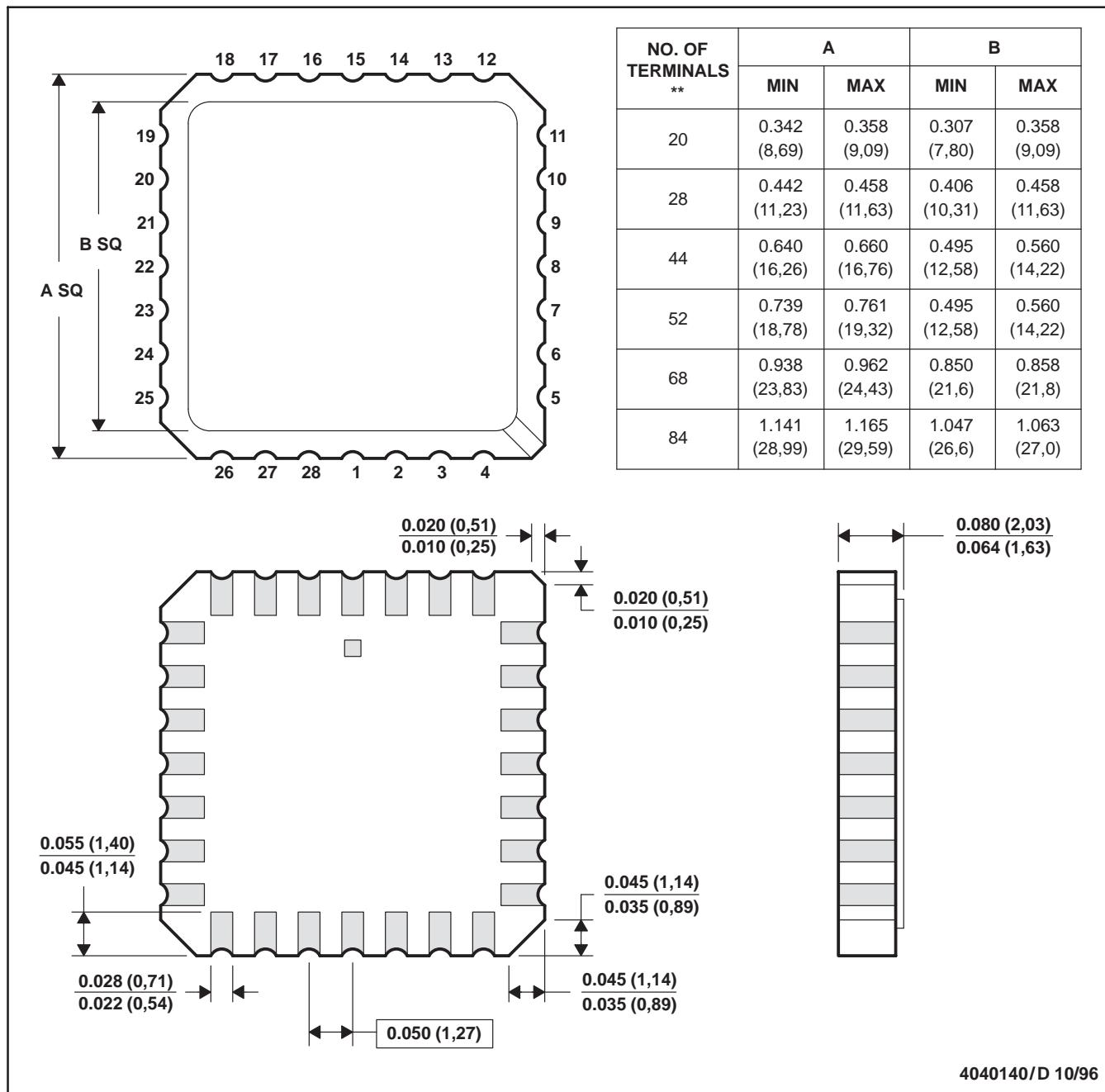
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



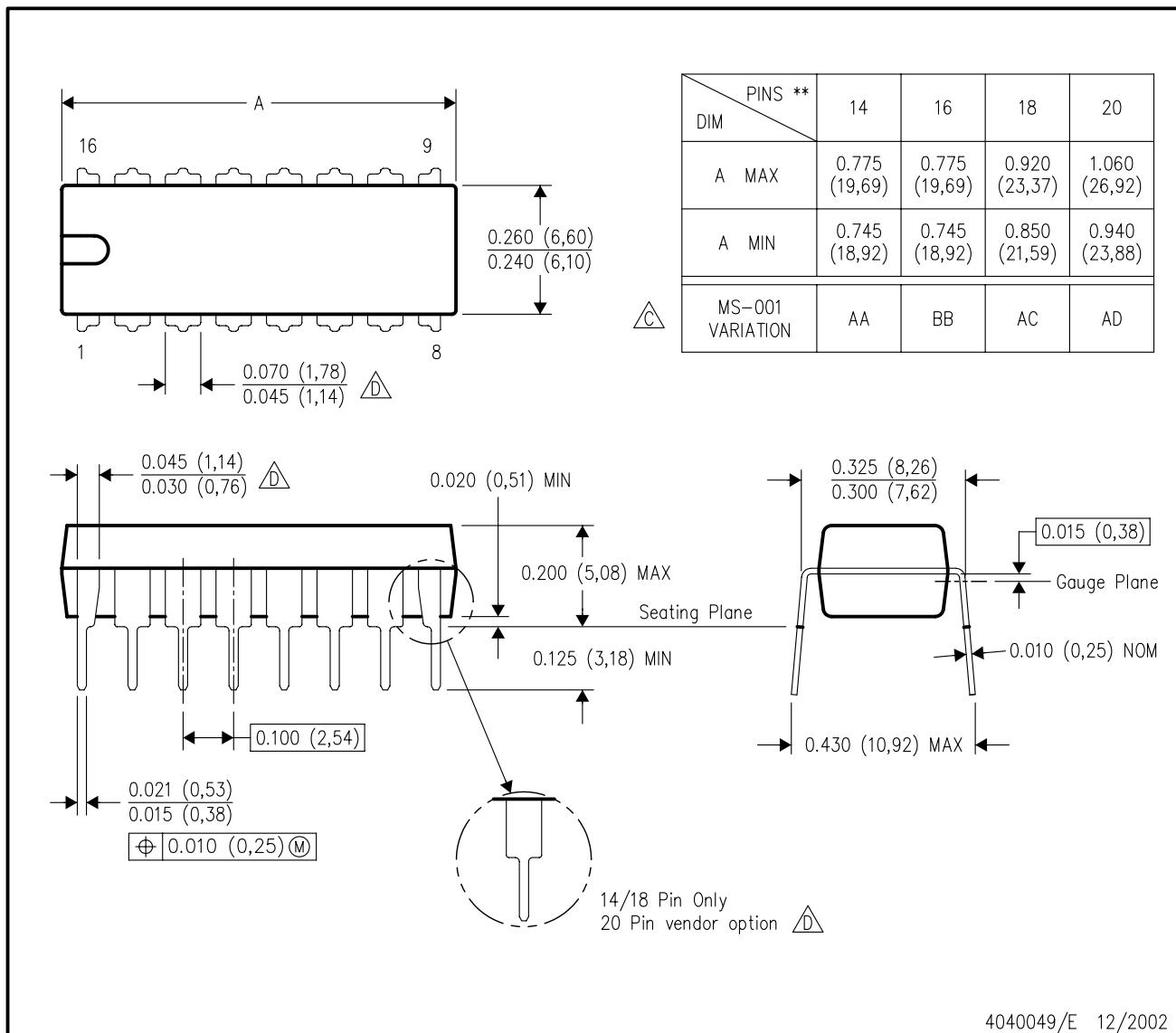
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

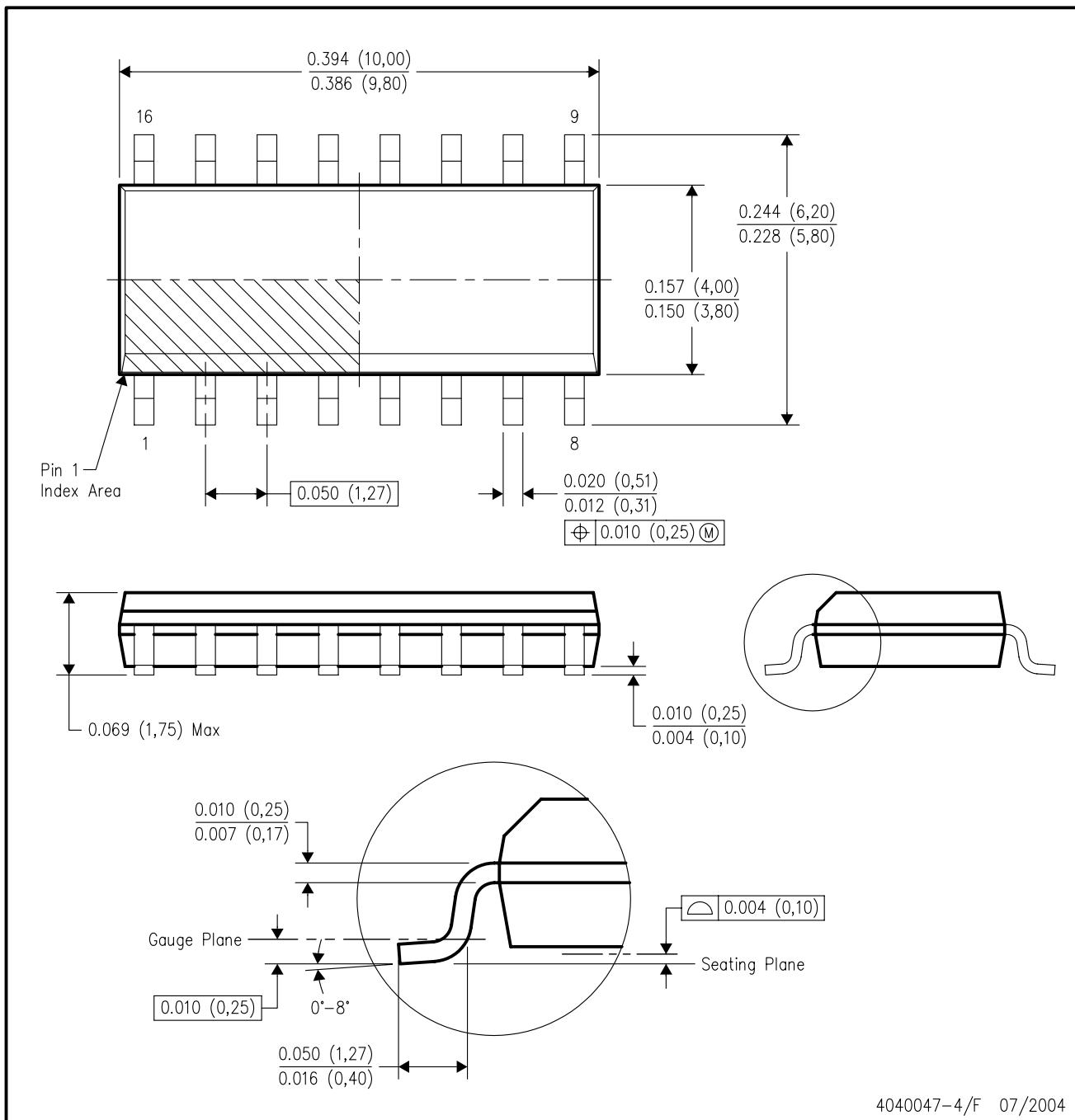
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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