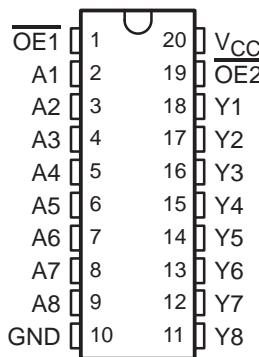
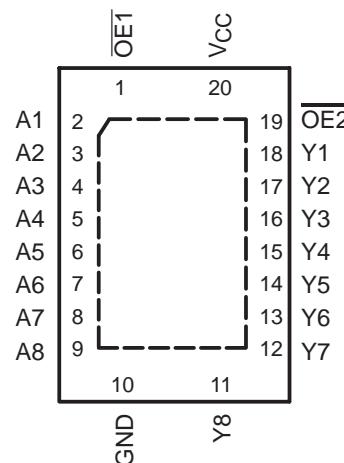


- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.1 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

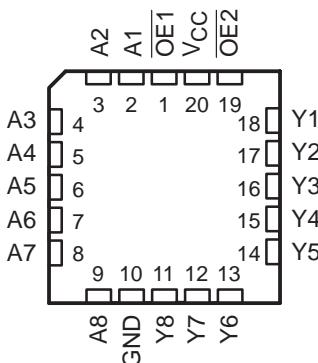
SN54LVC541A . . . J OR W PACKAGE  
SN74LVC541A . . . DB, DGV, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVC541A . . . RGY PACKAGE  
(TOP VIEW)



SN54LVC541A . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC541ARGYR
	SOIC – DW	Tube of 25	SN74LVC541ADW
		Reel of 2000	SN74LVC541ADWR
	SOP – NS	Reel of 2000	SN74LVC541ANSR
	SSOP – DB	Reel of 2000	SN74LVC541ADBR
	TSSOP – PW	Tube of 70	SN74LVC541APW
		Reel of 2000	SN74LVC541APWR
		Reel of 250	SN74LVC541APWT
–55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LVC541ADGVR
	CDIP – J	Tube of 20	SNJ54LVC541AJ
	CFP – W	Tube of 85	SNJ54LVC541AW
	LCCC – FK	Tube of 55	SNJ54LVC541AFK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LVC541A, SN74LVC541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS298M – JANUARY 1993 – REVISED AUGUST 2003

## description/ordering information (continued)

The SN54LVC541A octal buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC541A octal buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The 'LVC541A devices are ideal for driving bus lines or buffering memory address registers.

These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

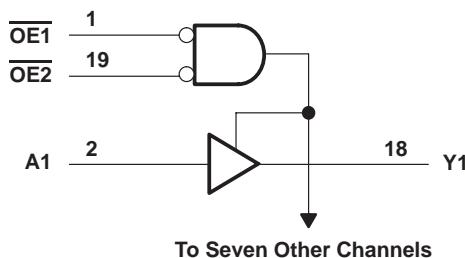
These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table. 3. The package thermal impedance is calculated in accordance with JESD 51-7. 4. The package thermal impedance is calculated in accordance with JESD 51-5.

**SN54LVC541A, SN74LVC541A  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 5)**

		SN54LVC541A		SN74LVC541A		UNIT	
		MIN	MAX	MIN	MAX		
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.65 × V <sub>CC</sub>		V	
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.7			
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		V	
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7			
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	0.8			
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state	0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V			-4	mA	
		V <sub>CC</sub> = 2.3 V			-8		
		V <sub>CC</sub> = 2.7 V	-12		-12		
		V <sub>CC</sub> = 3 V	-24		-24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V			4	mA	
		V <sub>CC</sub> = 2.3 V			8		
		V <sub>CC</sub> = 2.7 V	12		12		
		V <sub>CC</sub> = 3 V	24		24		
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC541A			SN74LVC541A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	1.65 V to 3.6 V				V <sub>CC</sub> -0.2			V
		2.7 V to 3.6 V	V <sub>CC</sub> -0.2						
	I <sub>OH</sub> = -4 mA	1.65 V				1.2			
	I <sub>OH</sub> = -8 mA	2.3 V				1.7			
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I <sub>OH</sub> = -24 mA	3 V	2.2			2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V				0.2	V		
		2.7 V to 3.6 V		0.2					
	I <sub>OL</sub> = 4 mA	1.65 V				0.45			
	I <sub>OL</sub> = 8 mA	2.3 V				0.7			
	I <sub>OL</sub> = 12 mA	2.7 V		0.4		0.4			
	I <sub>OL</sub> = 24 mA	3 V		0.55		0.55			
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V		±5		±5	µA		
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0				±10	µA		
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V		±15		±10	µA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND 3.6 V ≤ V <sub>I</sub> ≤ 5.5 V‡	I <sub>O</sub> = 0	3.6 V		10		10	µA	
					10		10		
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND		2.7 V to 3.6 V		500		500	µA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4		4	pF		
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5.5		5.5	pF		

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC541A				UNIT	
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			
			MIN	MAX	MIN	MAX		
t <sub>pd</sub>	A	Y			5.6	1	5.1	ns
t <sub>en</sub>	OE	Y			7.5	1	7	ns
t <sub>dis</sub>	OE	Y			7.7	1	7	ns

**SN54LVC541A, SN74LVC541A  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

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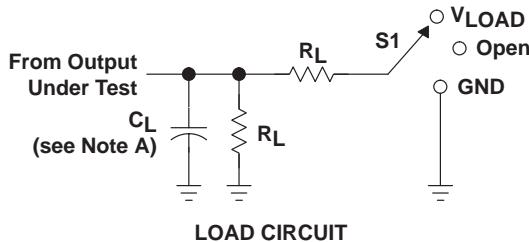
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC541A						UNIT		
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V				
			MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>pd</sub>	A	Y	1	15.7	1	7.8	1	5.6	1.5	5.1	
t <sub>en</sub>	OE	Y	1	17.5	1	10.5	1	7.5	1.5	7	
t <sub>dis</sub>	OE	Y	1	16.5	1	9	1	7.7	1.5	7	
t <sub>sk(o)</sub>									1	ns	

operating characteristics, T<sub>A</sub> = 25°C

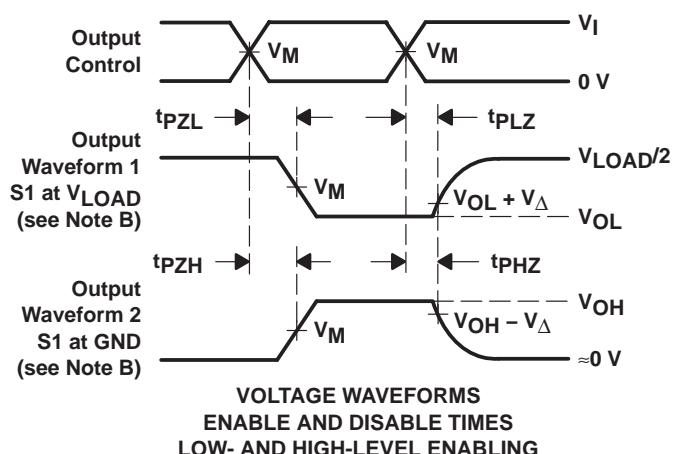
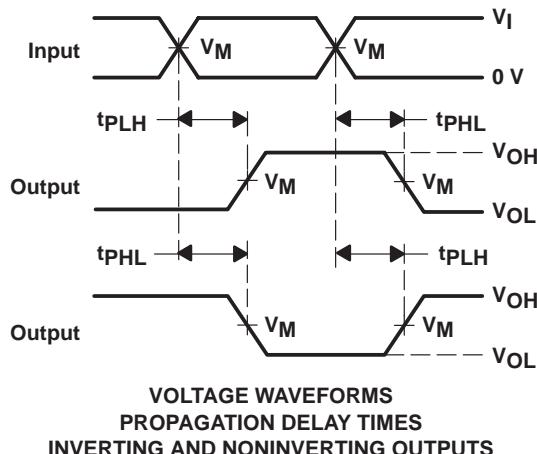
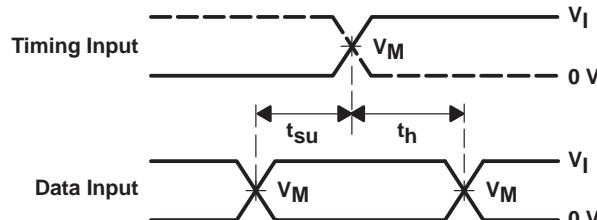
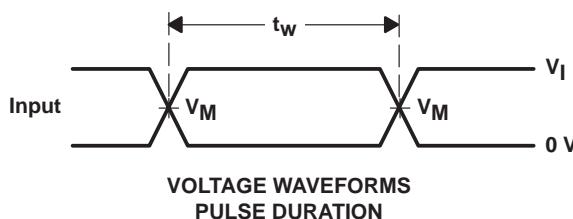
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT	
			TYP	TYP	TYP		
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	65	58	33	pF
		Outputs disabled		2	2	2	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8 V \pm 0.15 V$	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

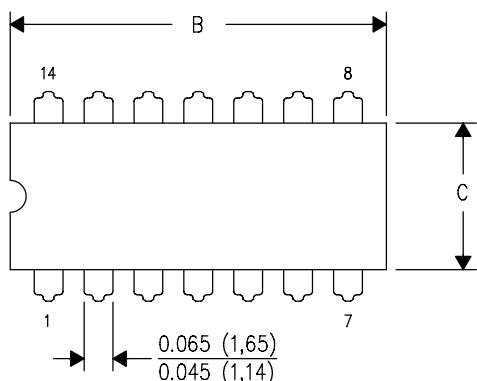
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

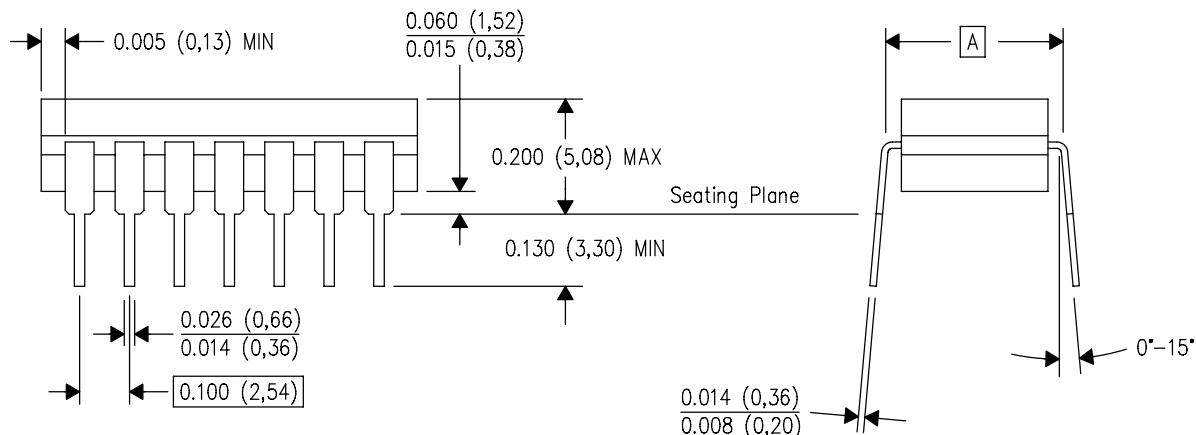
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

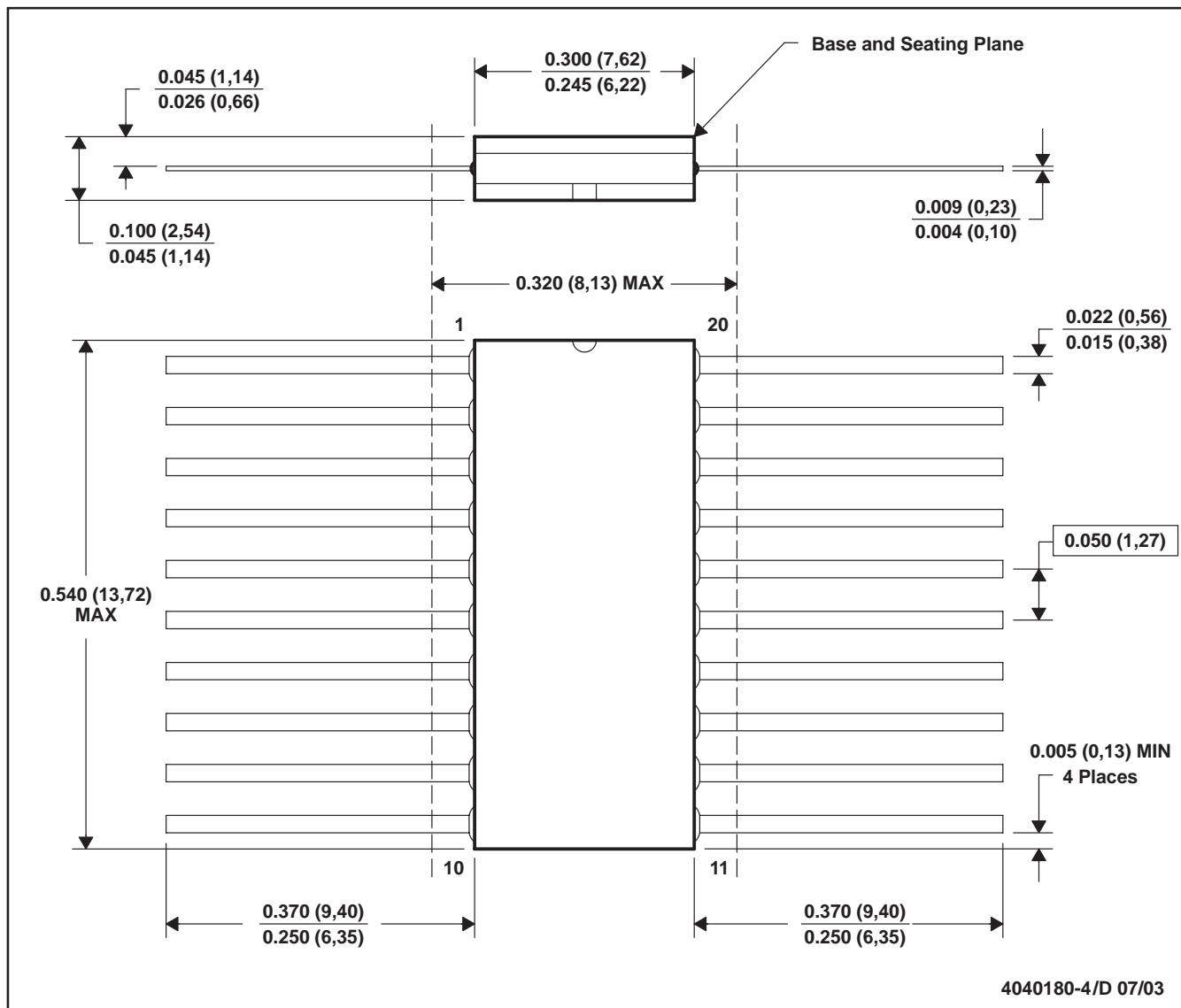


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



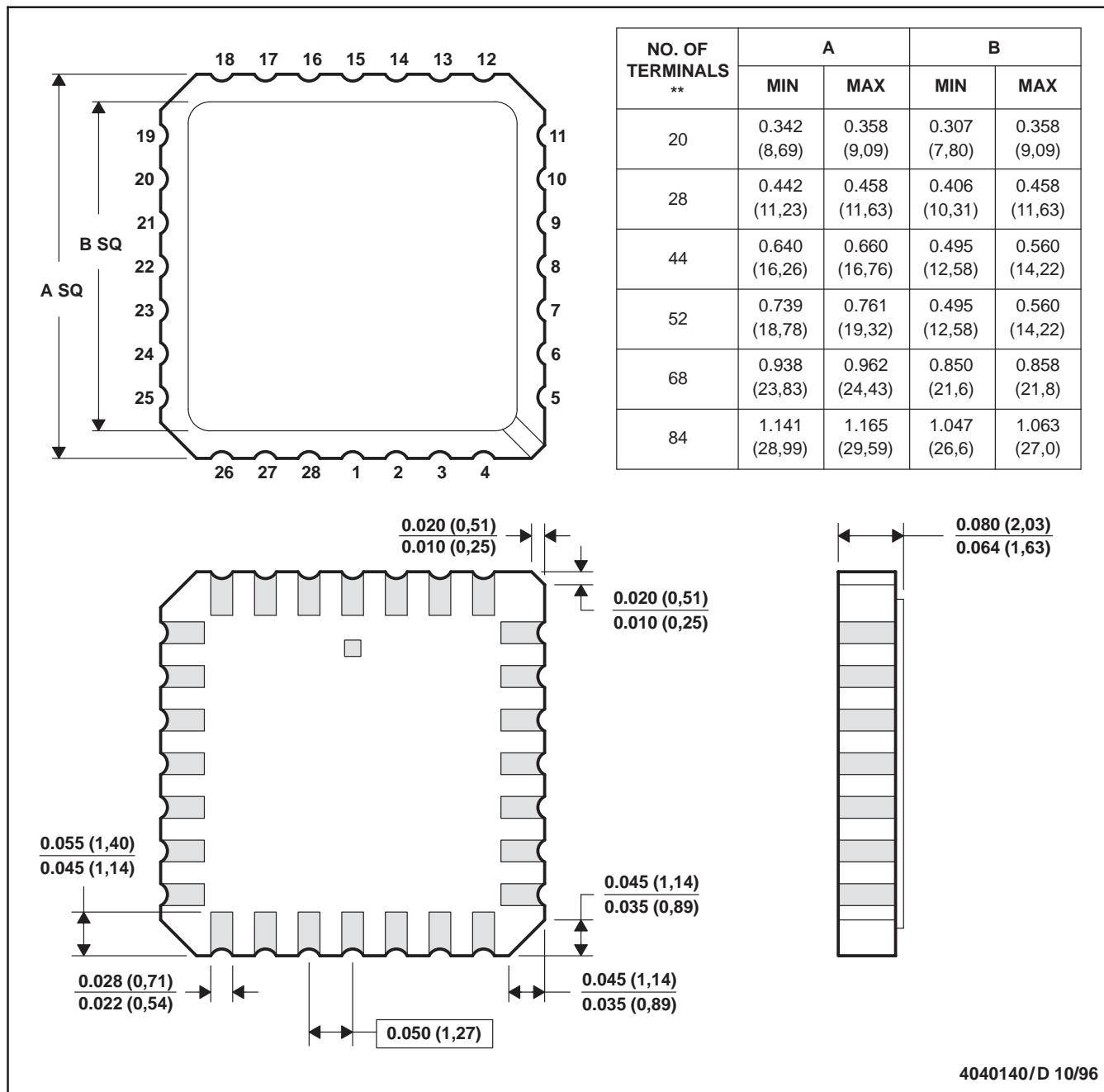
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within Mil-Std 1835 GDGP2-F20

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

## 28 TERMINAL SHOWN



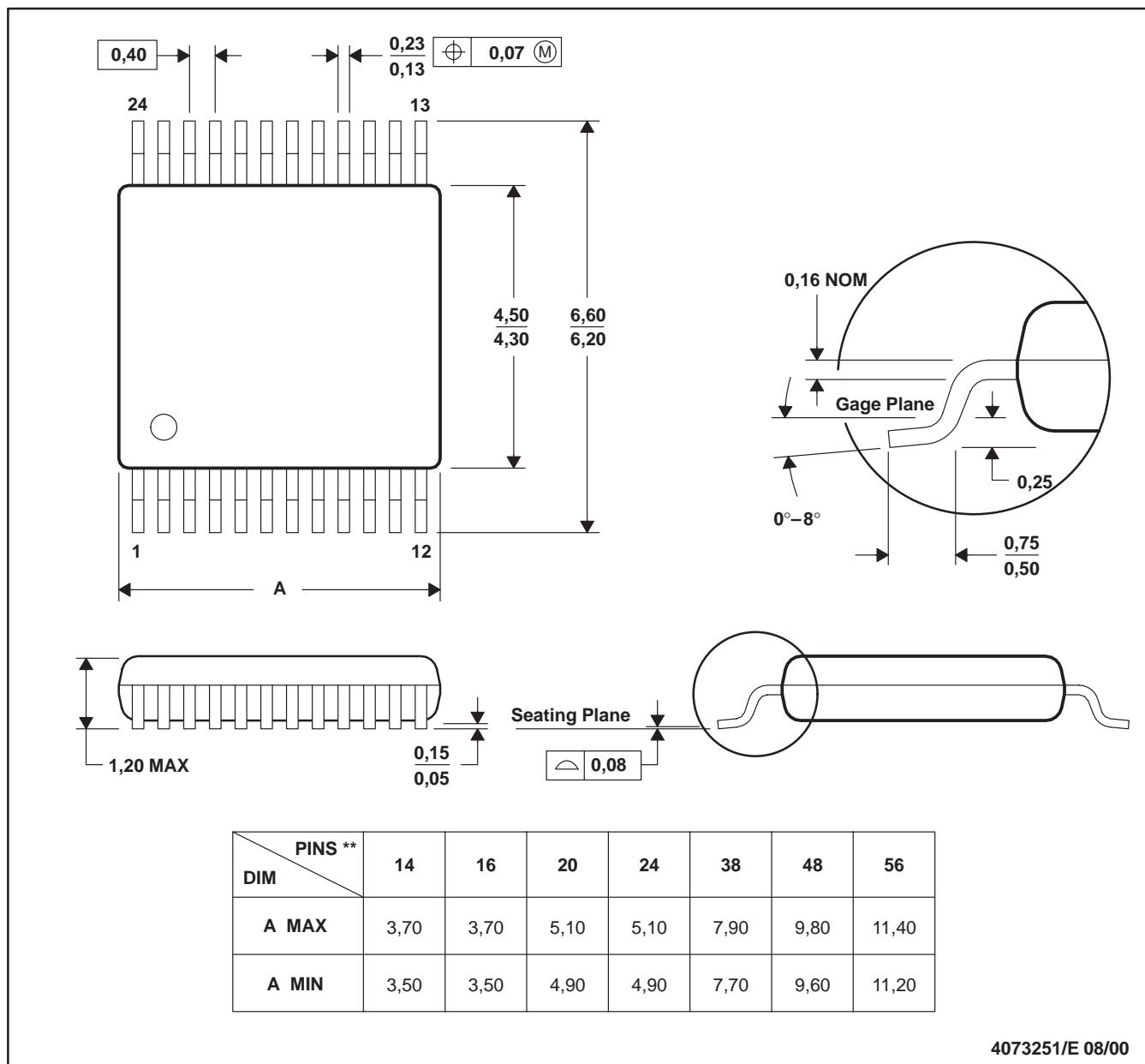
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

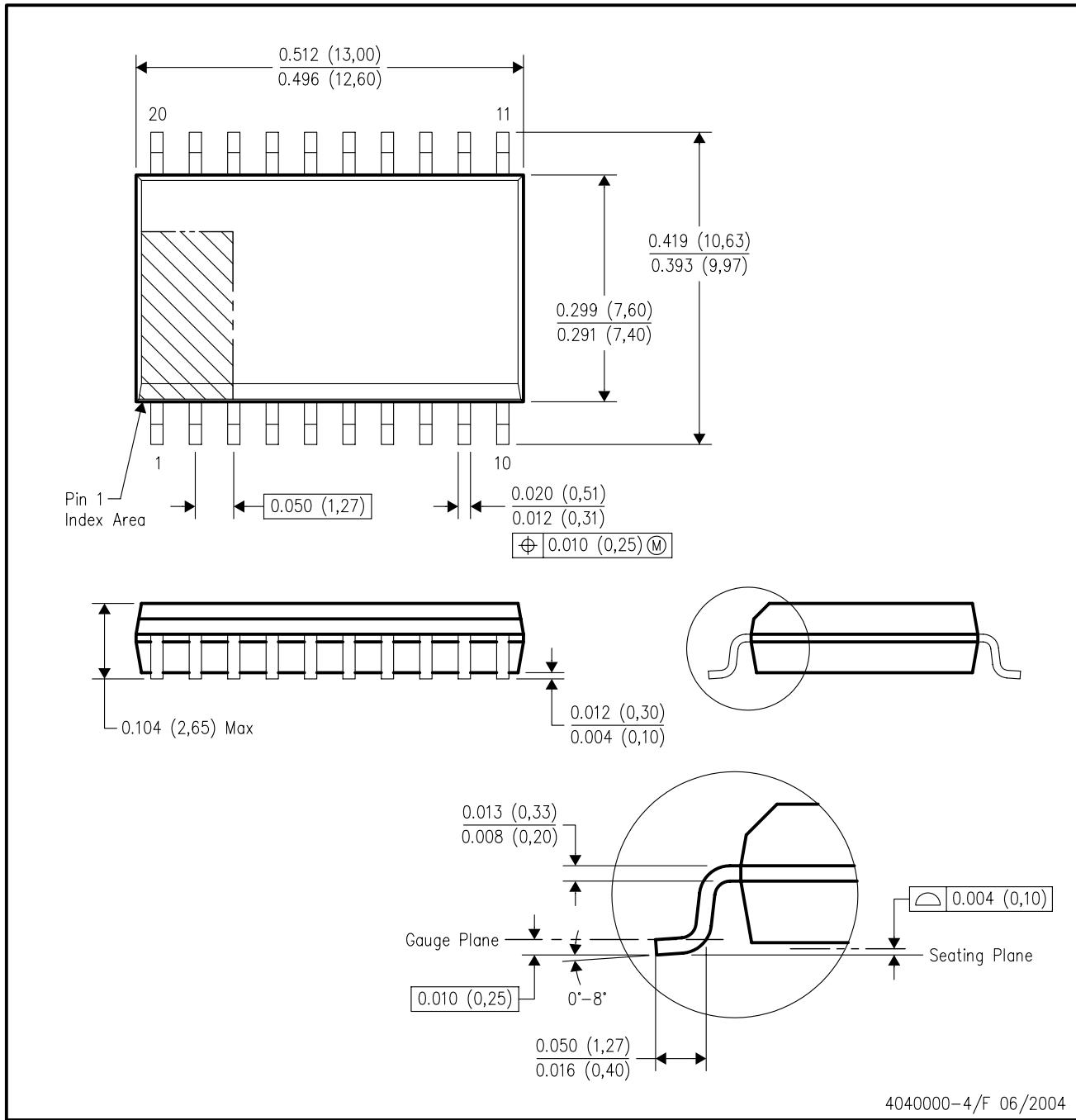
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE

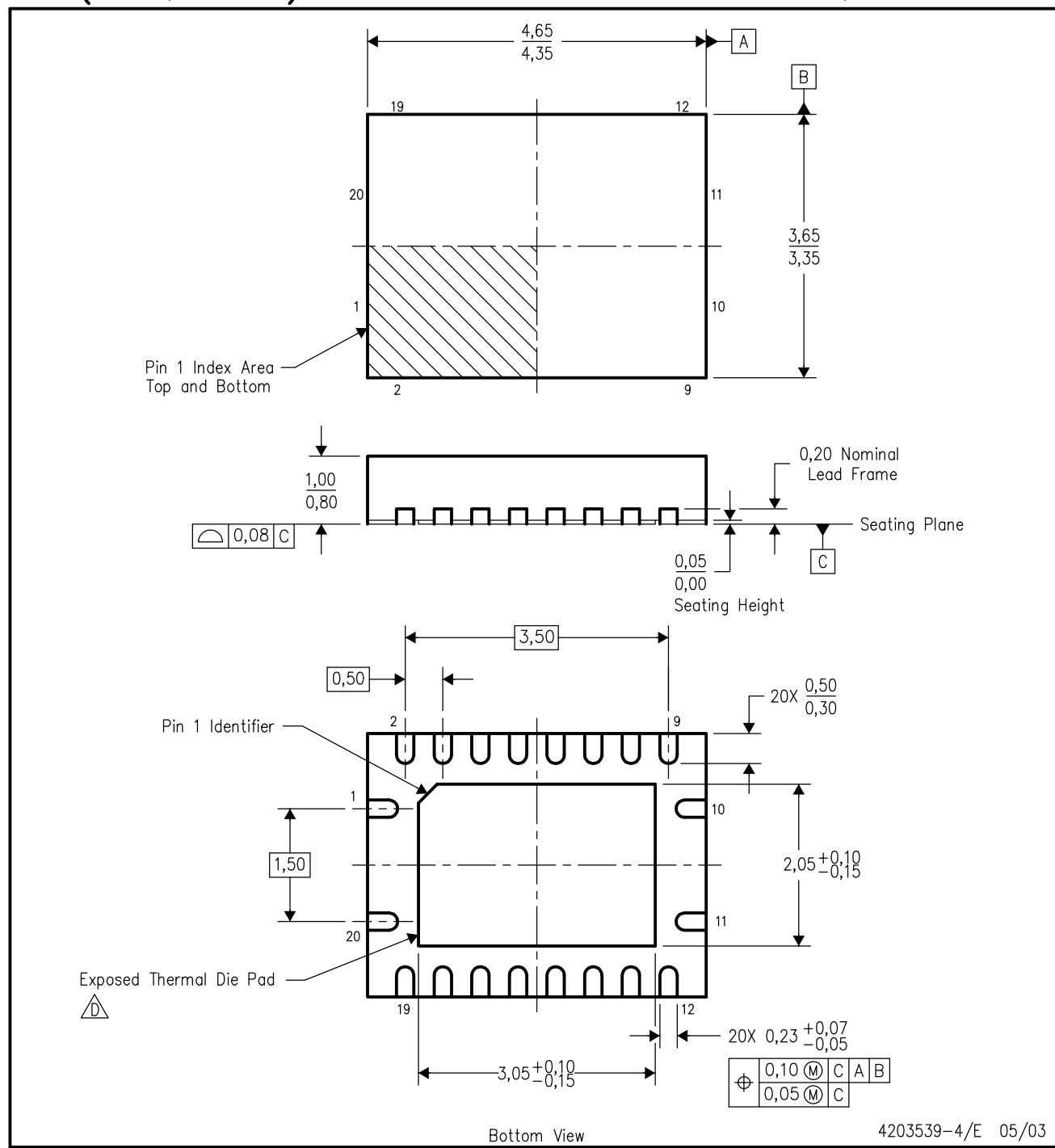


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



4203539-4/E 05/03

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

 The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.

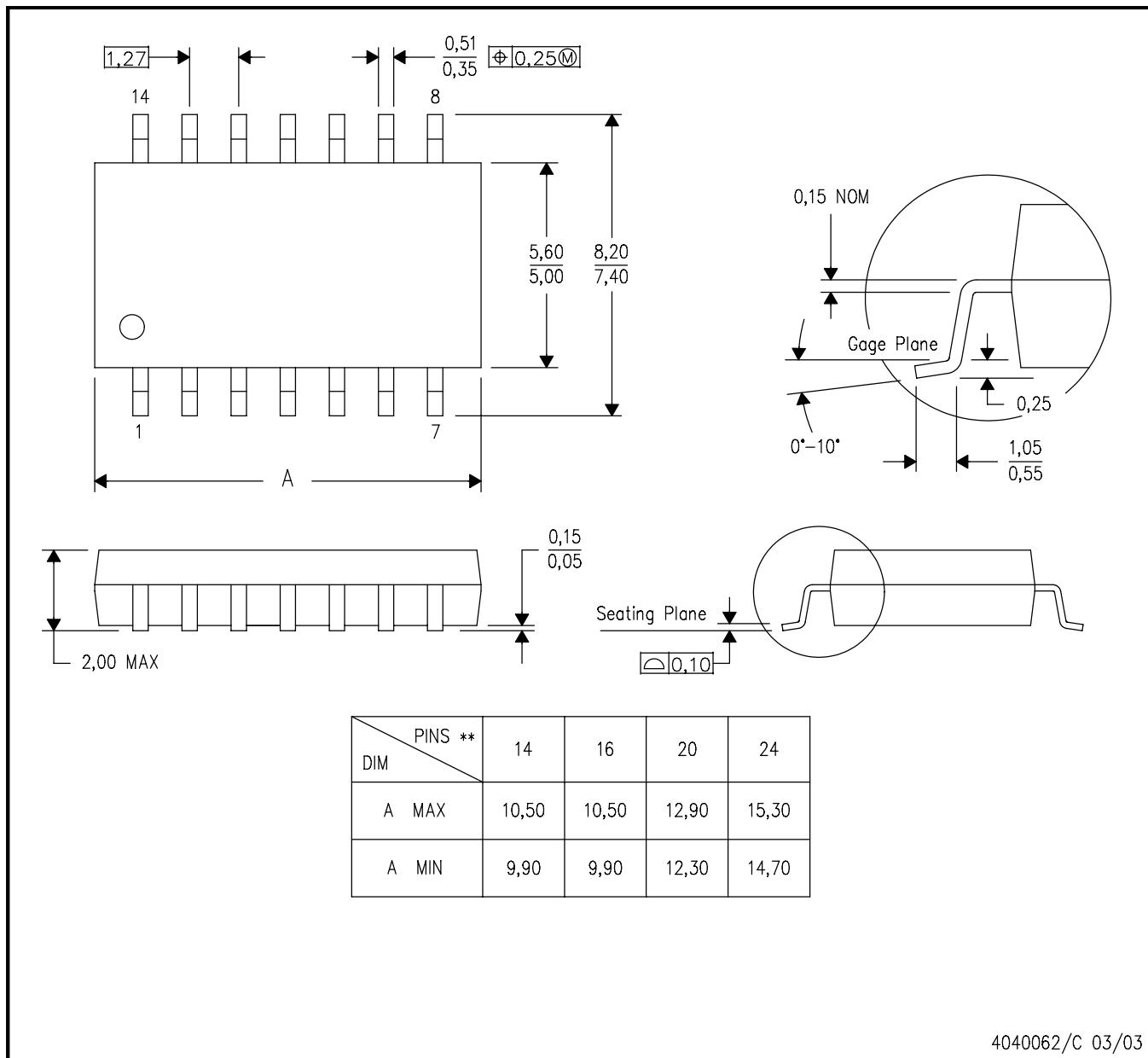
E. Package complies to JEDEC MO-241 variation BC.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



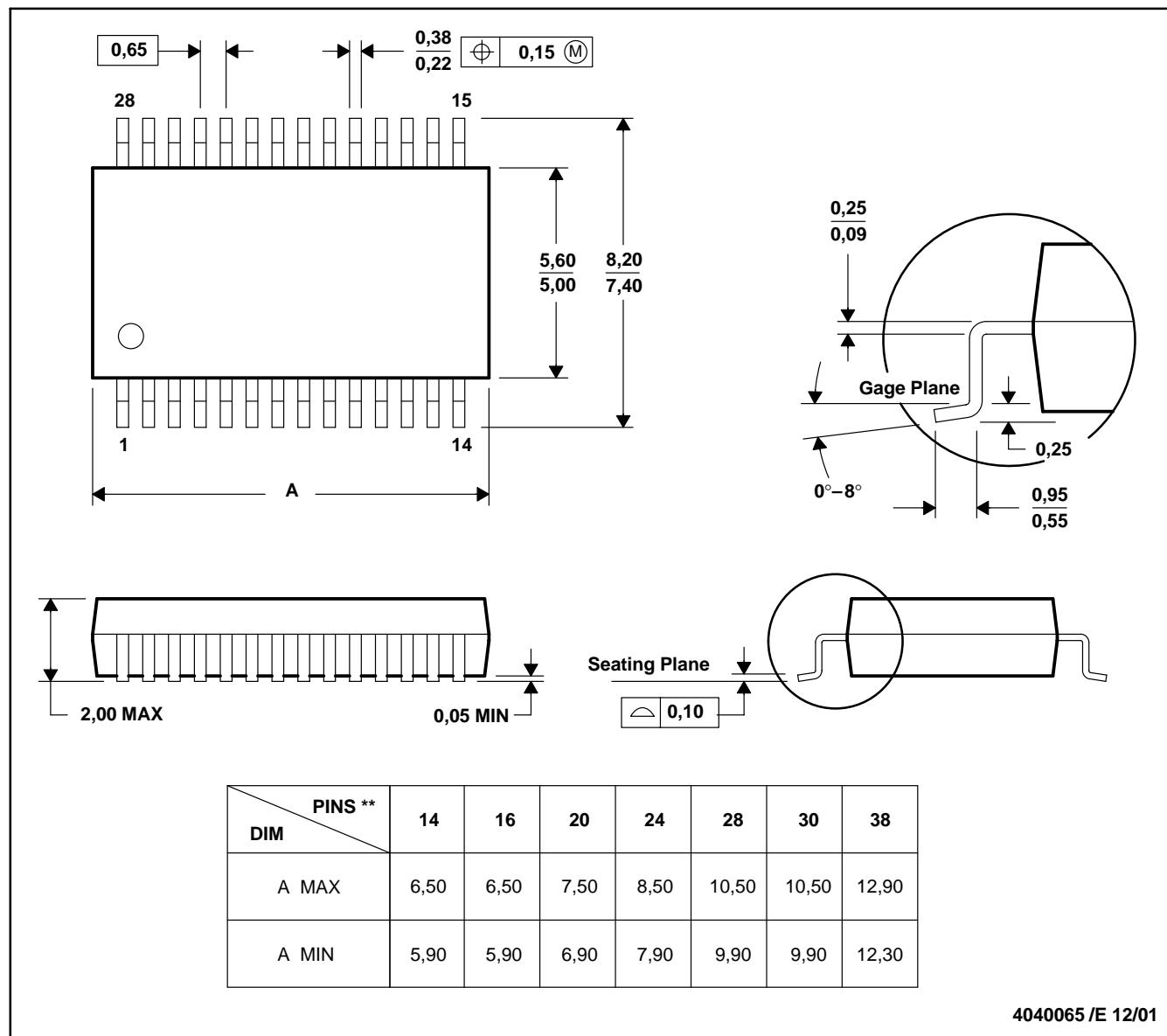
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

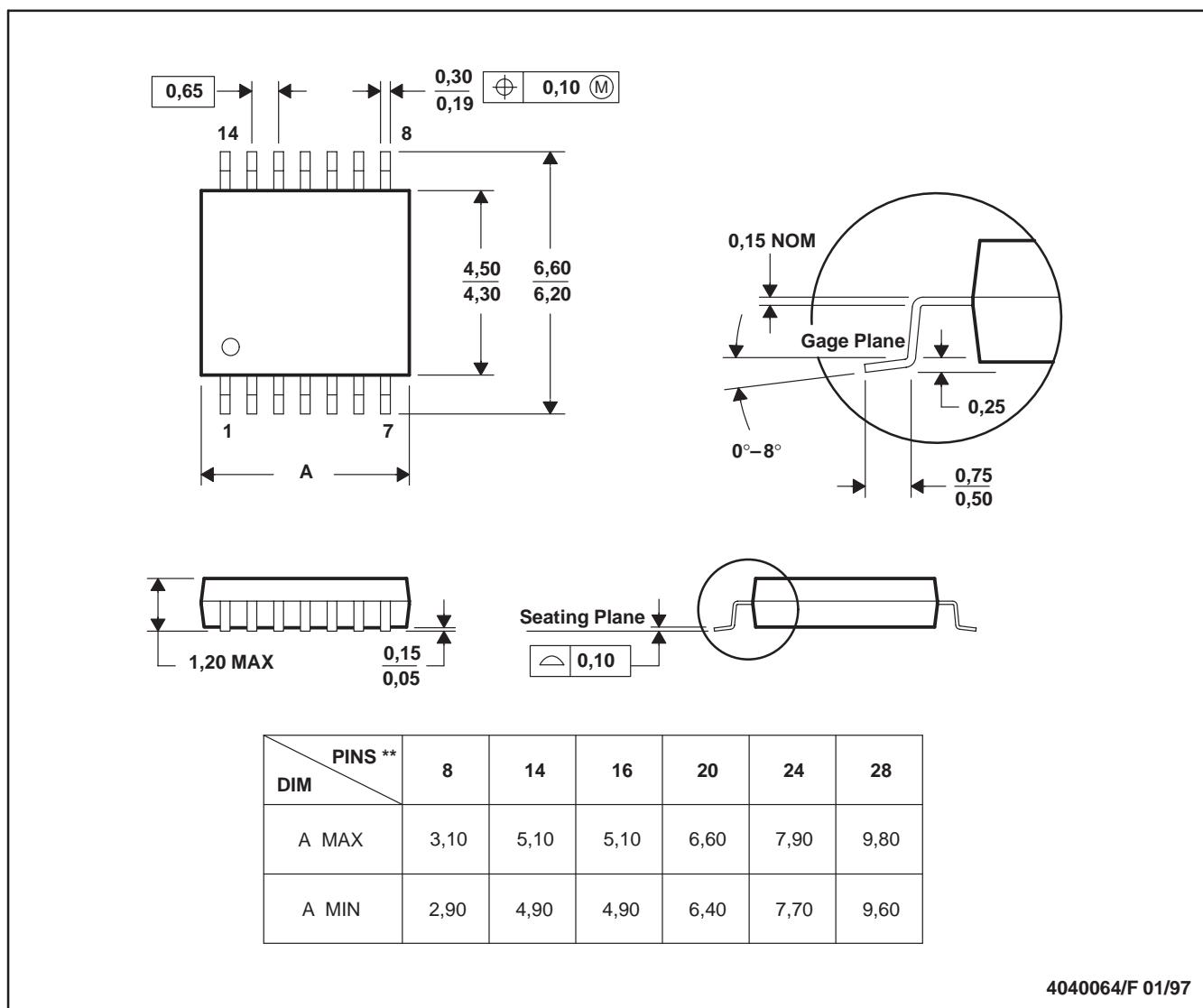


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

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