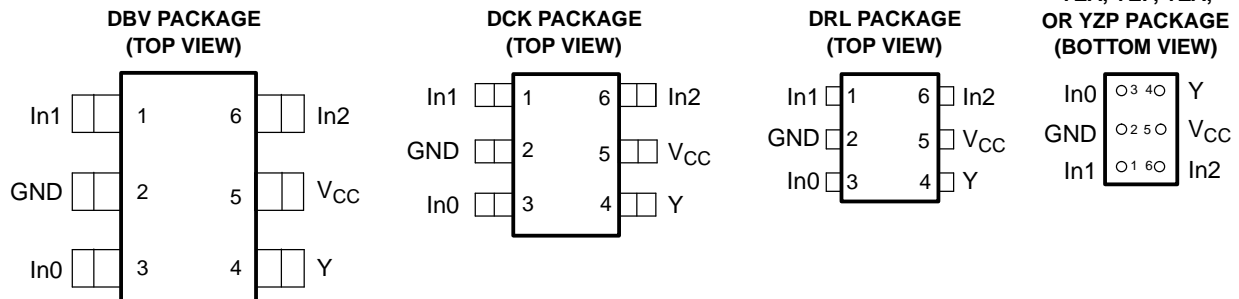


FEATURES

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.3 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G58 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XOR, inverter, and noninverter. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Tape and reel	SN74LVC1G58YEAR	___CP_
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		SN74LVC1G58YZAR	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LVC1G58YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G58YZPR	
	SOT (SOT-23) – DBV	Tape and reel	SN74LVC1G58DBVR	C58_
	SOT (SC-70) – DCK	Tape and reel	SN74LVC1G58DCKR	CP_
	SOT (SOT-563) – DRL	Reel of 4000	SN74LVC1G58DRLR	CP_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site. YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

SN74LVC1G58 CONFIGURABLE MULTIPLE-FUNCTION GATE

SCES415J–NOVEMBER 2002–REVISED MARCH 2006

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

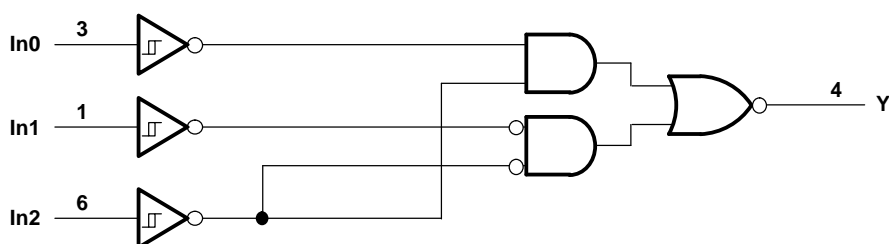
NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-input AND with inverted input	2, 3
2-input NAND	1
2-input NAND with both inputs inverted	4
2-input OR	4
2-input OR with both inputs inverted	1
2-input NOR with inverted input	2, 3
2-input XOR	5

LOGIC CONFIGURATIONS

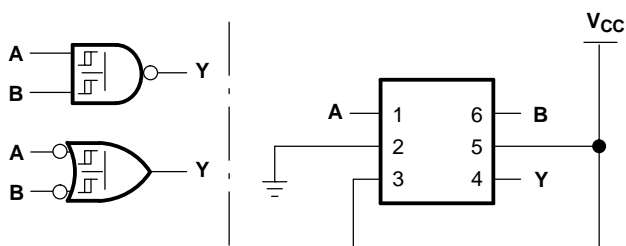


Figure 1. 2-Input NAND Gate

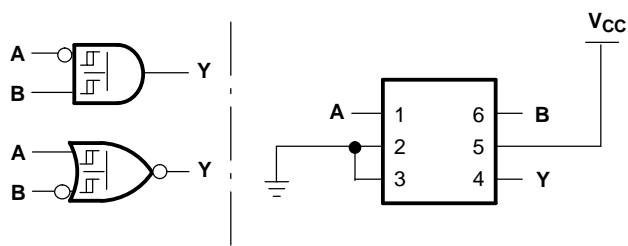


Figure 2. 2-Input AND Gate With Inverted A Input

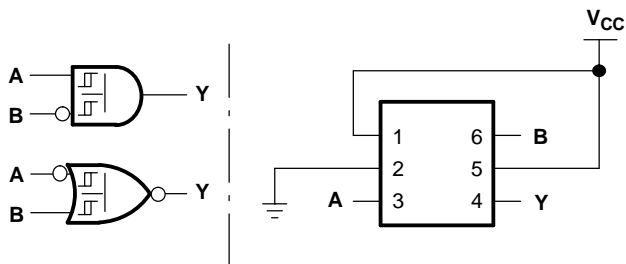


Figure 3. 2-Input AND Gate With Inverted B Input

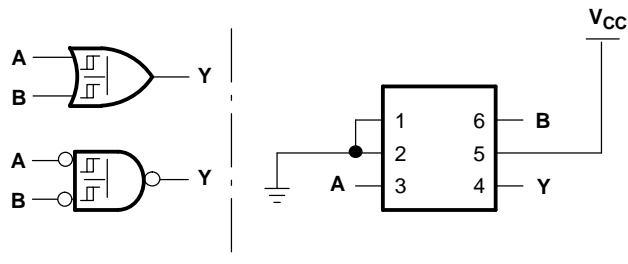


Figure 4. 2-Input OR Gate

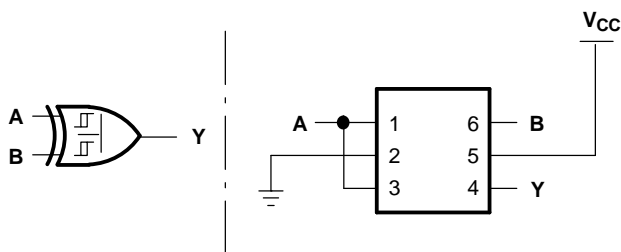


Figure 5. 2-Input XOR Gate

SN74LVC1G58

CONFIGURABLE MULTIPLE-FUNCTION GATE

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	6.5	V
V_I	Input voltage range ⁽²⁾	–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–50 mA
I_{OK}	Output clamp current	$V_O < 0$		–50 mA
I_O	Continuous output current			±50 mA
	Continuous current through V_{CC} or GND			±100 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DBV package		165
		DCK package		259
		DRL package		142
		YEA/YZA package		143
		YEP/YZP package		123
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating		V
		Data retention only		
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		mA
		V _{CC} = 2.3 V		
		V _{CC} = 3 V		
		V _{CC} = 4.5 V		
I _{OL}	Low-level output current	V _{CC} = 1.65 V		mA
		V _{CC} = 2.3 V		
		V _{CC} = 3 V		
		V _{CC} = 4.5 V		
T _A	Operating free-air temperature	−40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{T+} Positive-going input threshold voltage		1.65 V	0.79		1.16	V
		2.3 V	1.11		1.56	
		3 V	1.5		1.87	
		4.5 V	2.16		2.74	
		5.5 V	2.61		3.33	
V_{T-} Negative-going input threshold voltage		1.65 V	0.35		0.62	V
		2.3 V	0.58		0.87	
		3 V	0.84		1.19	
		4.5 V	1.41		1.9	
		5.5 V	1.87		2.29	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		1.65 V	0.3		0.62	V
		2.3 V	0.4		0.8	
		3 V	0.53		0.87	
		4.5 V	0.71		1.04	
		5.5 V	0.71		1.11	
V_{OH}	$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	$V_{CC} - 0.1$			V
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			
	$I_{OH} = -16 \text{ mA}$	3 V	2.4			
	$I_{OH} = -24 \text{ mA}$		2.3			
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
V_{OL}	$I_{OL} = 100 \mu A$	1.65 V to 5.5 V	0.1			V
	$I_{OL} = 4 \text{ mA}$	1.65 V	0.45			
	$I_{OL} = 8 \text{ mA}$	2.3 V	0.3			
	$I_{OL} = 16 \text{ mA}$	3 V	0.4			
	$I_{OL} = 24 \text{ mA}$		0.55			
	$I_{OL} = 32 \text{ mA}$	4.5 V	0.55			
I_I	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V	± 1			μA
I_{off}	$V_I \text{ or } V_O = 5.5 \text{ V}$	0	± 10			μA
I_{CC}	$V_I = 5.5 \text{ V or GND, } I_O = 0$	1.65 V to 5.5 V	10			μA
ΔI_{CC}	One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND	3 V to 5.5 V	500			μA
C_i	$V_I = V_{CC} \text{ or GND}$	3.3 V	3.5			pF

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

SN74LVC1G58

CONFIGURABLE MULTIPLE-FUNCTION GATE

SCES415J–NOVEMBER 2002–REVISED MARCH 2006

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Any In	Y	3.2	14.4	2	8.3	1.5	6.3	1.1	5.1	ns

Operating Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	22	22	23	24	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 6. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC1G58DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G58DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G58DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G58DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G58DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G58DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G58DRLR	ACTIVE	SOP	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G58DRLRG4	ACTIVE	SOP	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G58YEAR	NRND	WCSP	YEA	6	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G58YEPR	NRND	WCSP	YEP	6	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G58YZAR	NRND	WCSP	YZA	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1G58YZPR	ACTIVE	WCSP	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

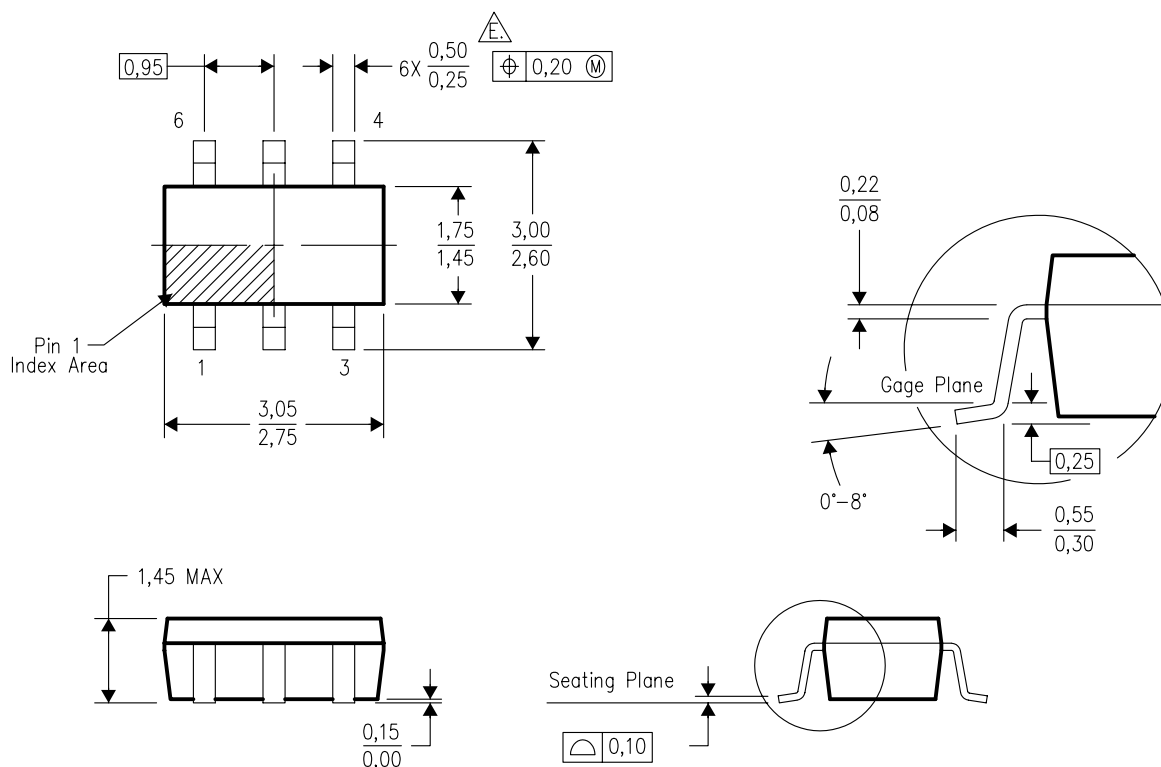
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DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

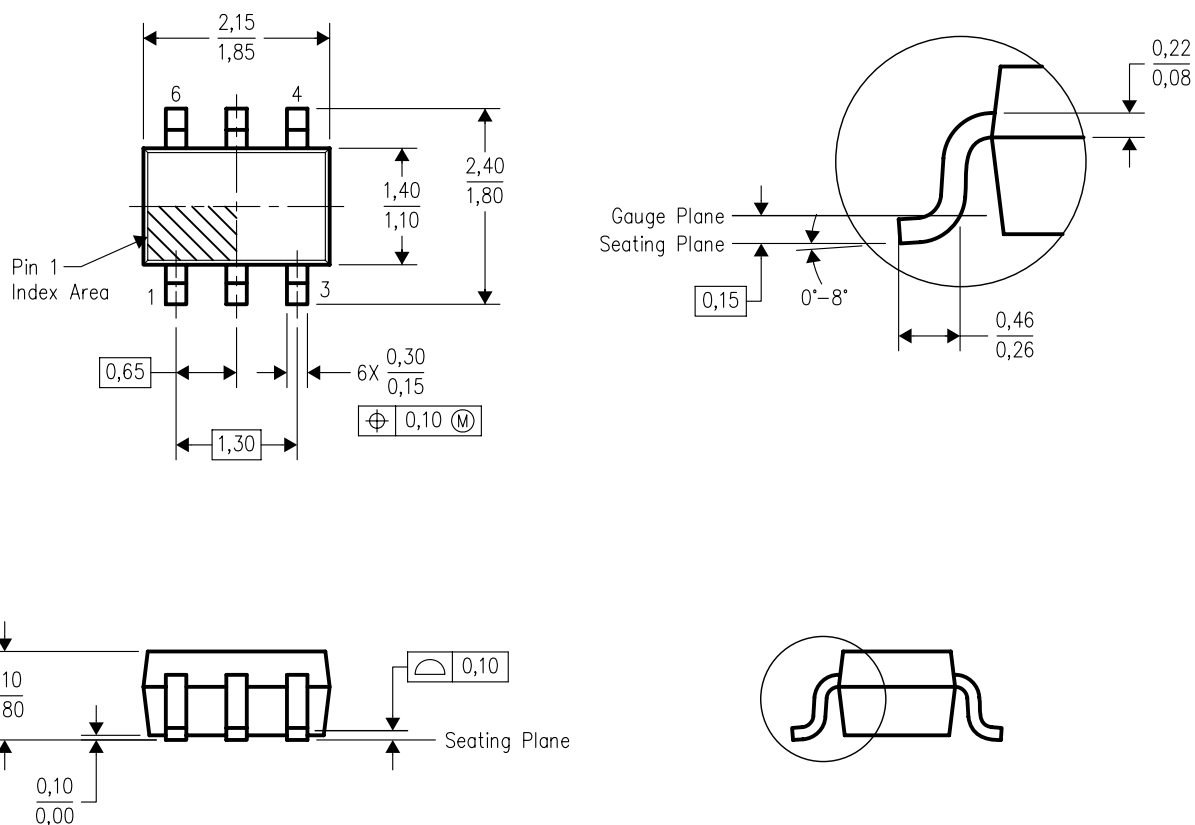


4073253-5/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- \triangle Falls within JEDEC MO-178 Variation AB, except minimum lead width.

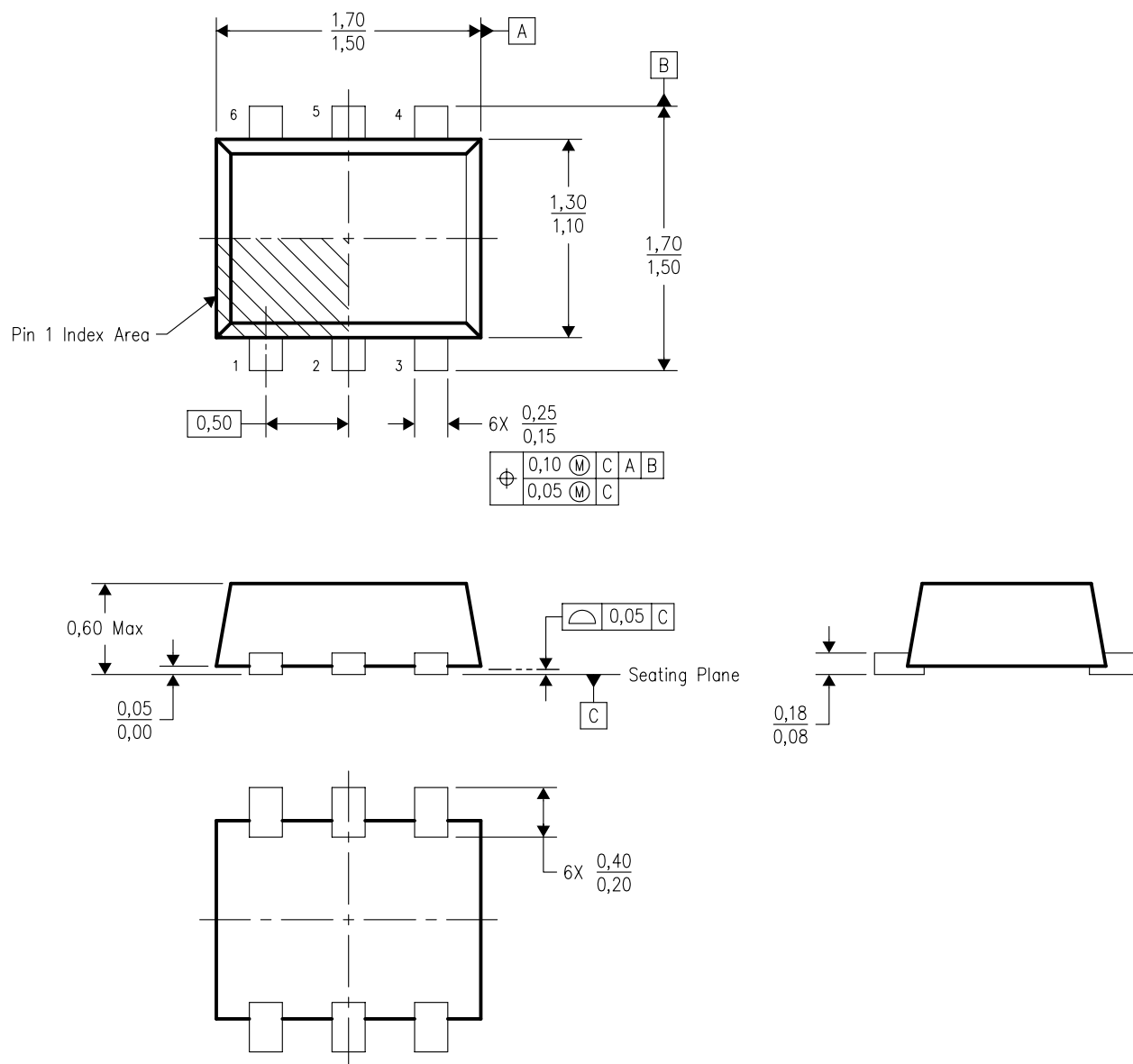
DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/F 07/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

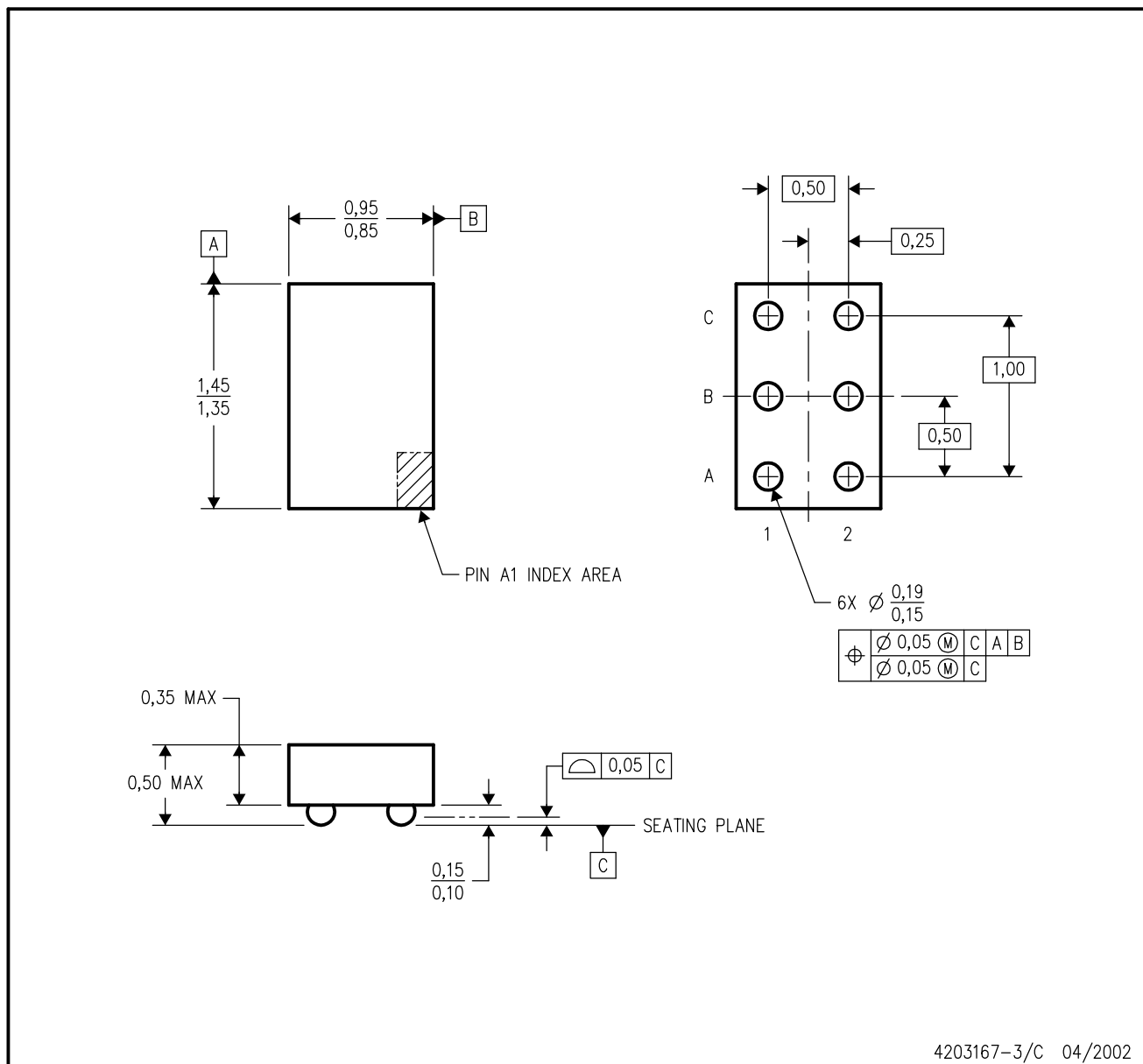


4205622-3/B 07/2004

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. JEDEC package registration is pending.

YEA (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY

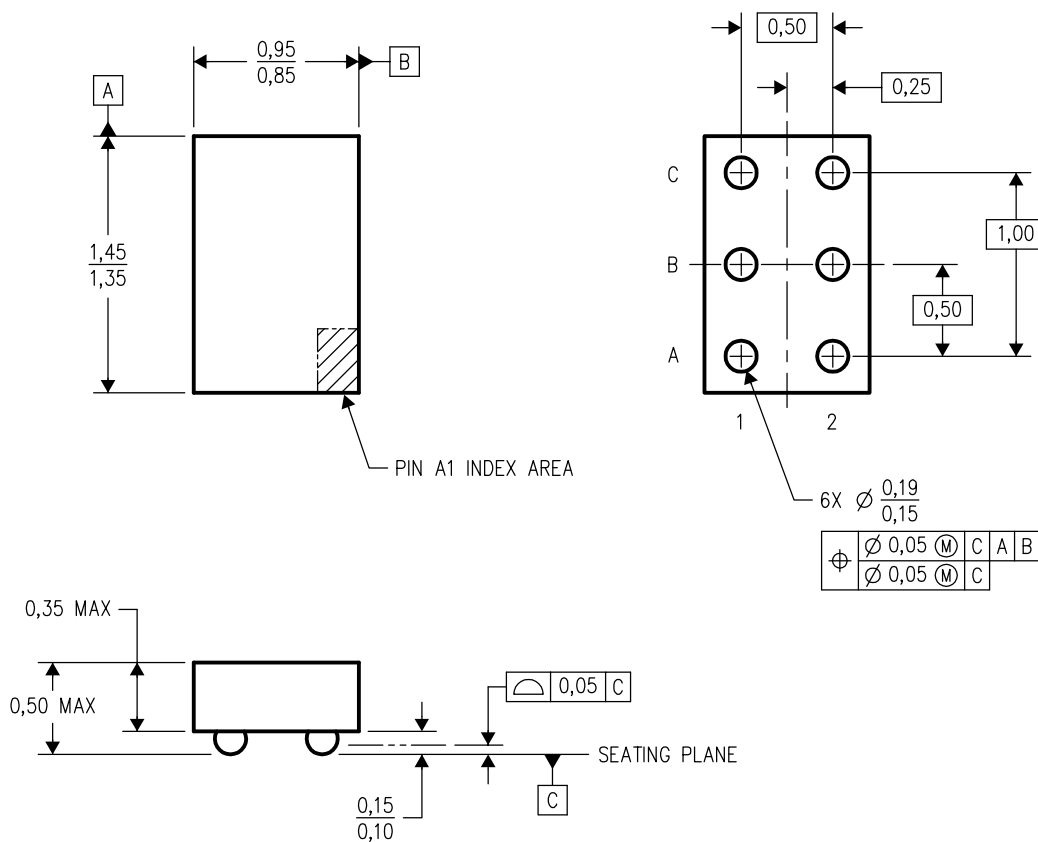


4203167-3/C 04/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is tin-lead (SnPb). Refer to the 6 YZA package (drawing 4204151) for lead-free.

YZA (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



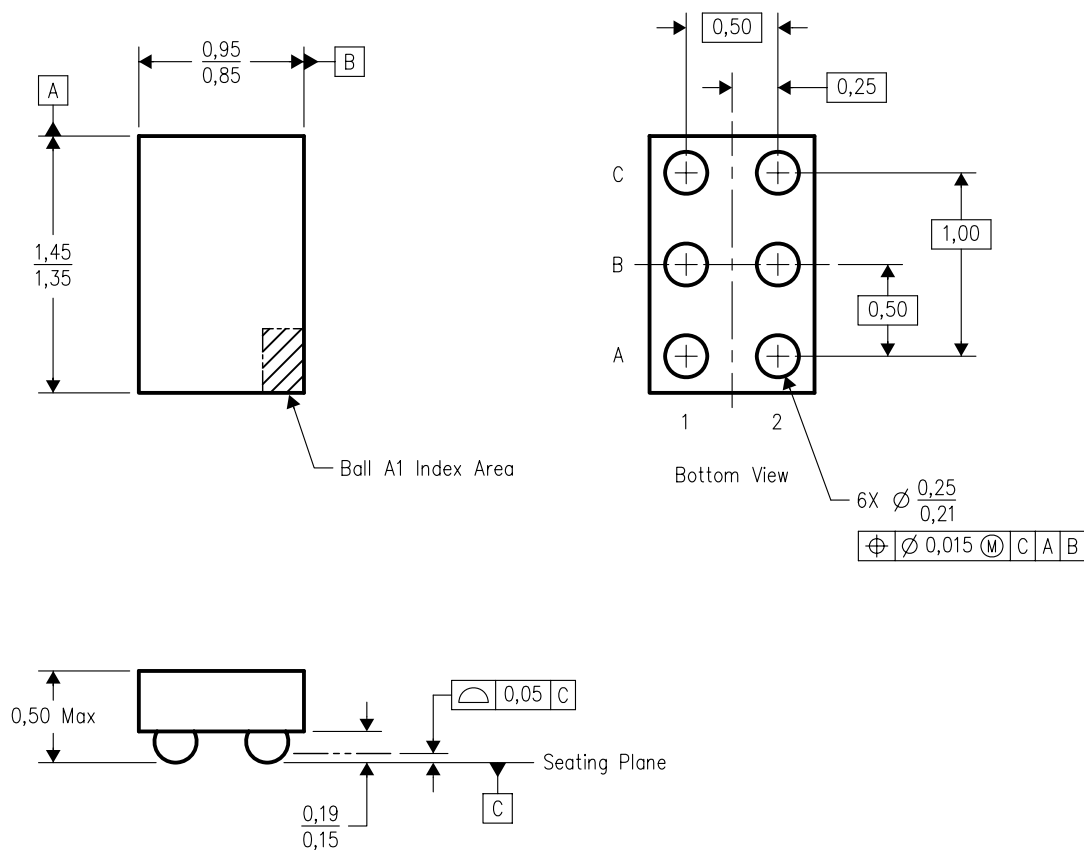
4204151-3/B 03/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is lead-free. Refer to the 6 YEA package (drawing 4203167) for tin-lead (SnPb).

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YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4204741-3/D 10/2006

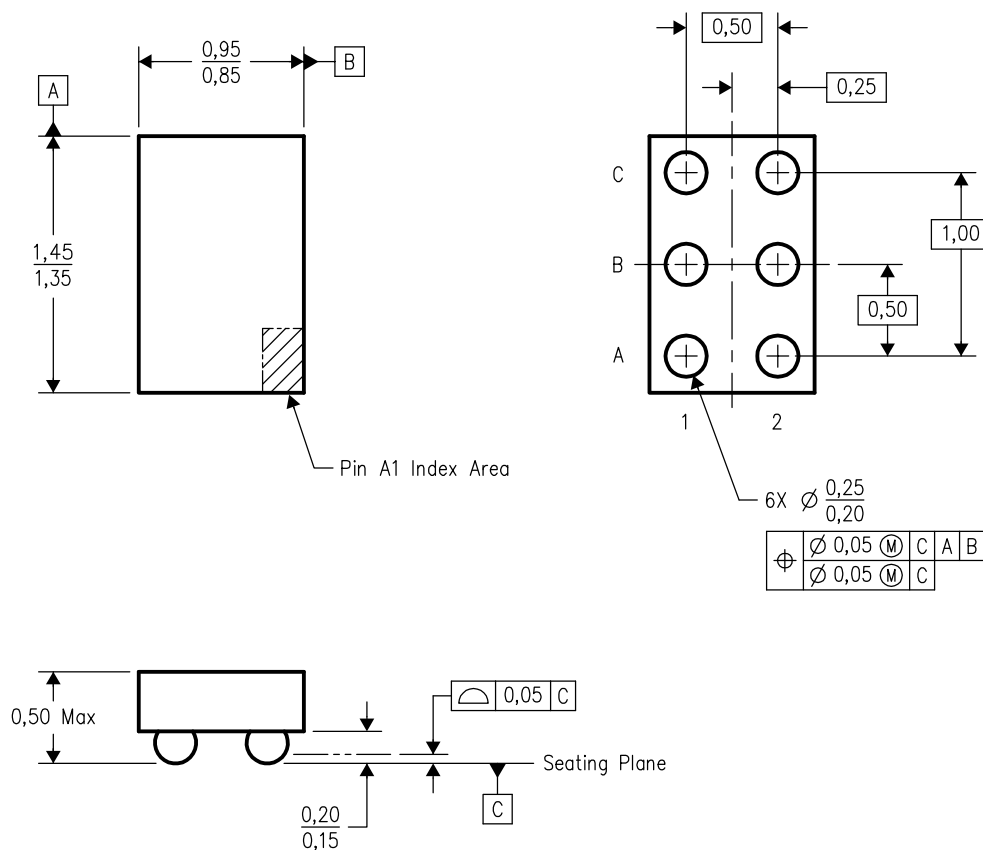
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead-free. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4204725-3/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead-free.

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