

SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS278 – JANUARY 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- True Logic
- 3-State Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

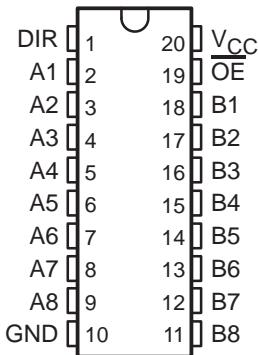
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

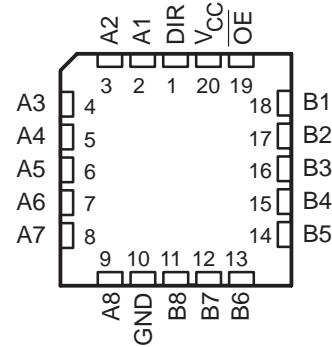
The -1 version of the SN74ALS645A is identical to the standard version, except that the recommended maximum I_{OL} is increased to 48 mA. There is no -1 version of the SN54ALS645A.

The SN54ALS645A and SN54AS645 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS645A and SN74AS645 are characterized for operation from 0°C to 70°C .

SN54ALS645A, SN54AS645 . . . J PACKAGE
SN74ALS645A, SN74AS645 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS645A, SN54AS645 . . . FK PACKAGE
(TOP VIEW)



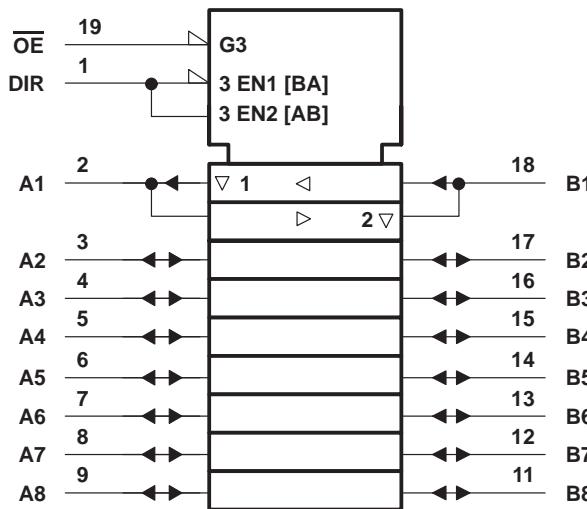
FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

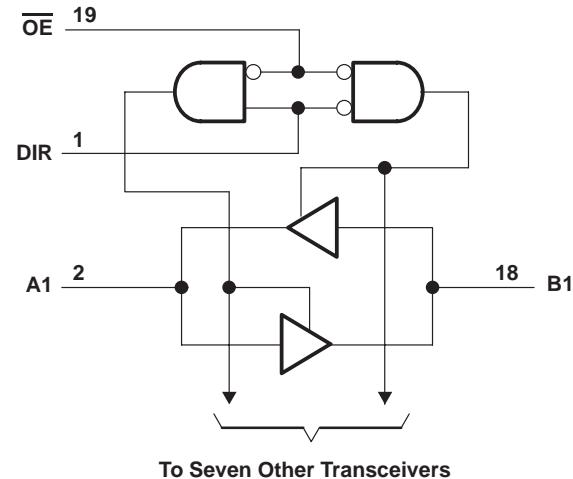
SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54ALS645A	-55°C to 125°C
SN74ALS645A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS645A			SN74ALS645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2		2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			12			24	mA
							48§	
T _A	Operating free-air temperature	-55		125	0		70	°C

§ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS645A			SN74ALS645A			UNIT
		MIN	TYPT†	MAX	MIN	TYPT†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -12 \text{ mA}$	2					
		$I_{OH} = -15 \text{ mA}$				2		
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
		$I_{OL} = 48 \text{ mA}^{\ddagger}$			0.35	0.5		
I_I	Control inputs	$V_I = 7 \text{ V}$		0.1		0.1		mA
	A or B ports	$V_I = 5.5 \text{ V}$		0.1		0.1		
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$		20		20		μA
	A or B ports \S			20		20		
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.1		-0.1		mA
	A or B ports \S			-0.1		-0.1		
$I_{O\ddagger}$	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-20	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	30	48	30	45		mA
		Outputs low	36	60	36	55		
		Outputs disabled	38	63	38	58		

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\#}$				UNIT	
			SN54ALS645A		SN74ALS645A			
			MIN	MAX	MIN	MAX		
t_{PLH}	A or B	B or A	1	19	3	10	ns	
t_{PHL}			1	14	3	10		
t_{PZH}	\overline{OE}	A or B	2	30	5	20	ns	
t_{PZL}			2	29	5	20		
t_{PHZ}	\overline{OE}	A or B	2	14	2	10	ns	
t_{PLZ}			2	30	4	15		

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS645			SN74AS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2		2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			48			64	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS645			SN74AS645			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -12 \text{ mA}$	2.4					
		$I_{OH} = -15 \text{ mA}$			2.4			
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 48 \text{ mA}$	0.3	0.55				V
		$I_{OL} = 64 \text{ mA}$				0.35	0.55	
I_I	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 7 \text{ V}$		0.1		0.1	mA
	A or B ports		$V_I = 5.5 \text{ V}$		0.1		0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 2.7 \text{ V}$		20		20	μA
	A or B ports§				70		70	
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 0.4 \text{ V}$		-0.5		-0.5	mA
	A or B ports§				-0.75		-0.75	
I_O ¶	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$		-50	-150	-50	-150	mA	
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	62	97	62	97		mA
		Outputs low	95	149	95	149		
		Outputs disabled	79	123	79	123		

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{SC} .

switching characteristics (see Figure 1)

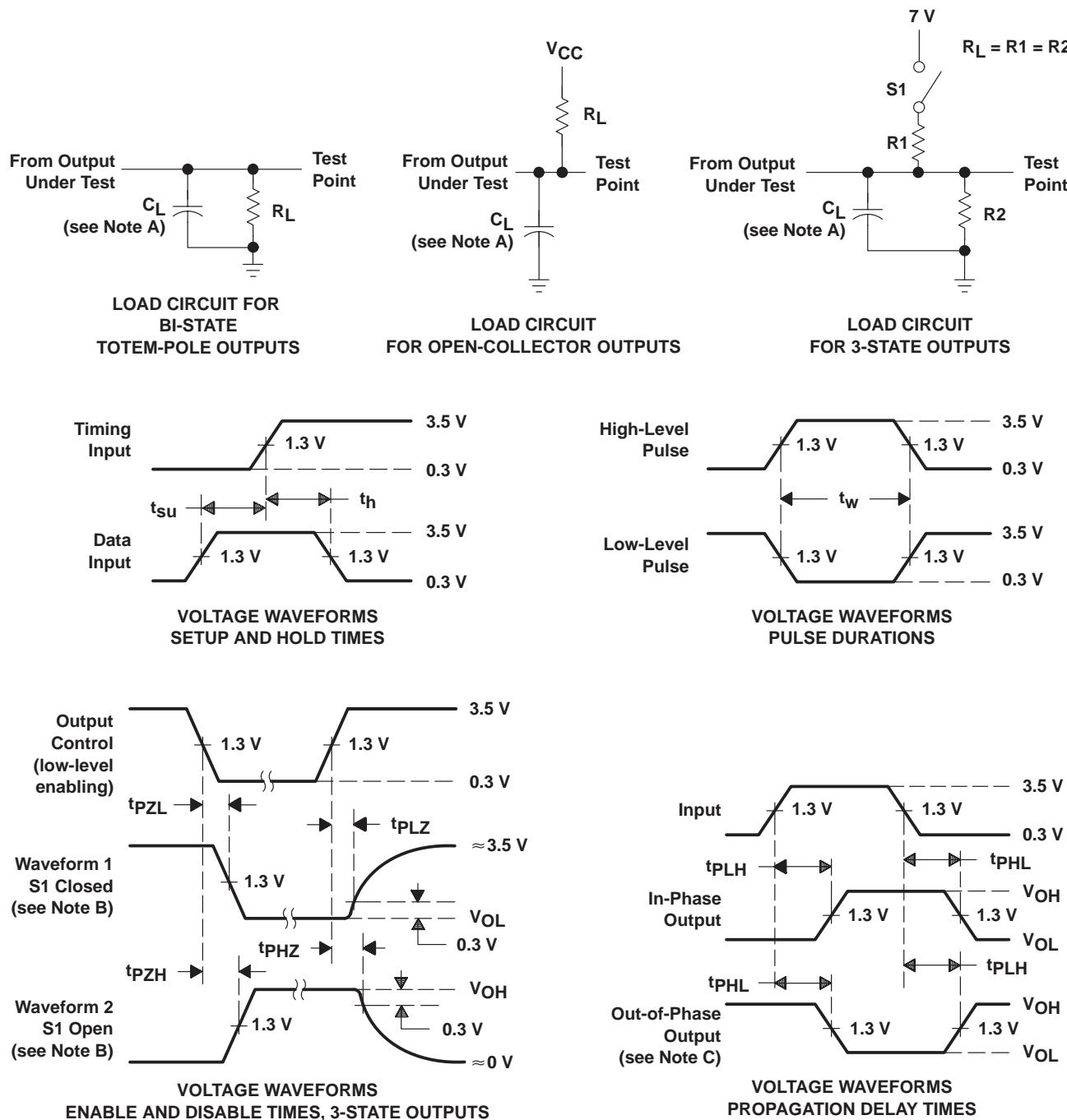
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R1 = 500\text{ }\Omega$, $R2 = 500\text{ }\Omega$, $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54AS645		SN74AS645			
			MIN	MAX	MIN	MAX		
t_{PLH}	A or B	B or A	2	11	2	9.5	ns	
t_{PHL}			2	10.5	2	9		
t_{PZH}	\overline{OE}	A or B	2	12	2	11	ns	
t_{PZL}			2	12	2	10		
t_{PHZ}	\overline{OE}	A or B	2	8	2	7	ns	
t_{PLZ}			2	13	2	12		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
84033012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
8403301RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
8403301SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN54ALS645AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54AS645J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN74ALS645A-1DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS645A-1DWE4	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS645A-1DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS645A-1DWRE4	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS645A-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS645A-1N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SN74ALS645A-1NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS645A-1NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS645A-1NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS645ADW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS645ADWE4	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS645ADWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS645ADWRE4	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS645AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS645AN3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SN74ALS645ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS645ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS645ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS645DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74AS645DWE4	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74AS645DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74AS645DWRE4	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74AS645N	ACTIVE	PDIP	N	20	20	Pb-Free	CU NIPDAU	Level-NC-NC-NC

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
(RoHS)								
SN74AS645NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ54ALS645AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ALS645AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ALS645AW	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54AS645FK	OBsolete	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54AS645J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54AS645W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

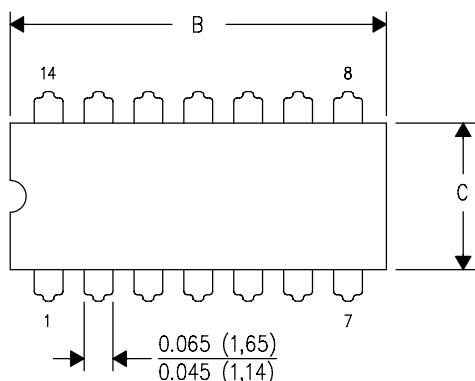
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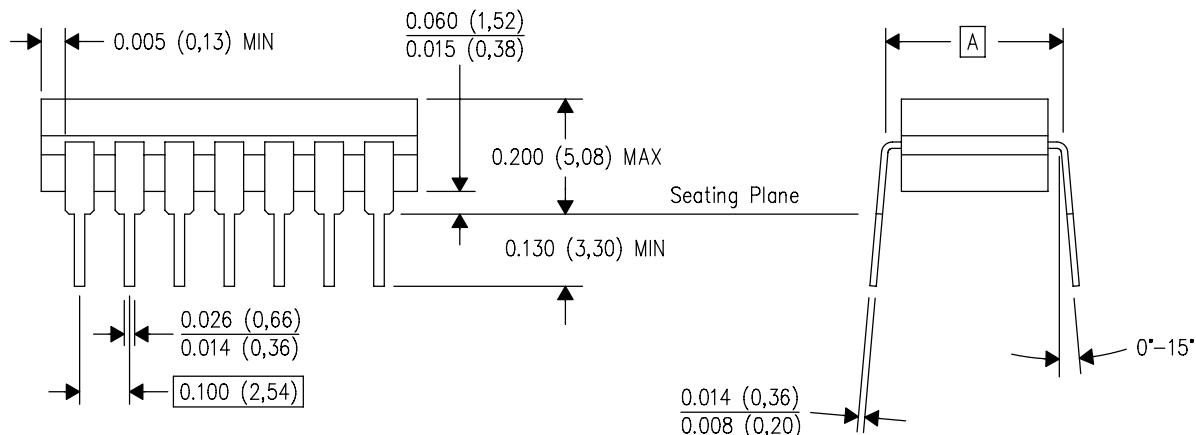
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

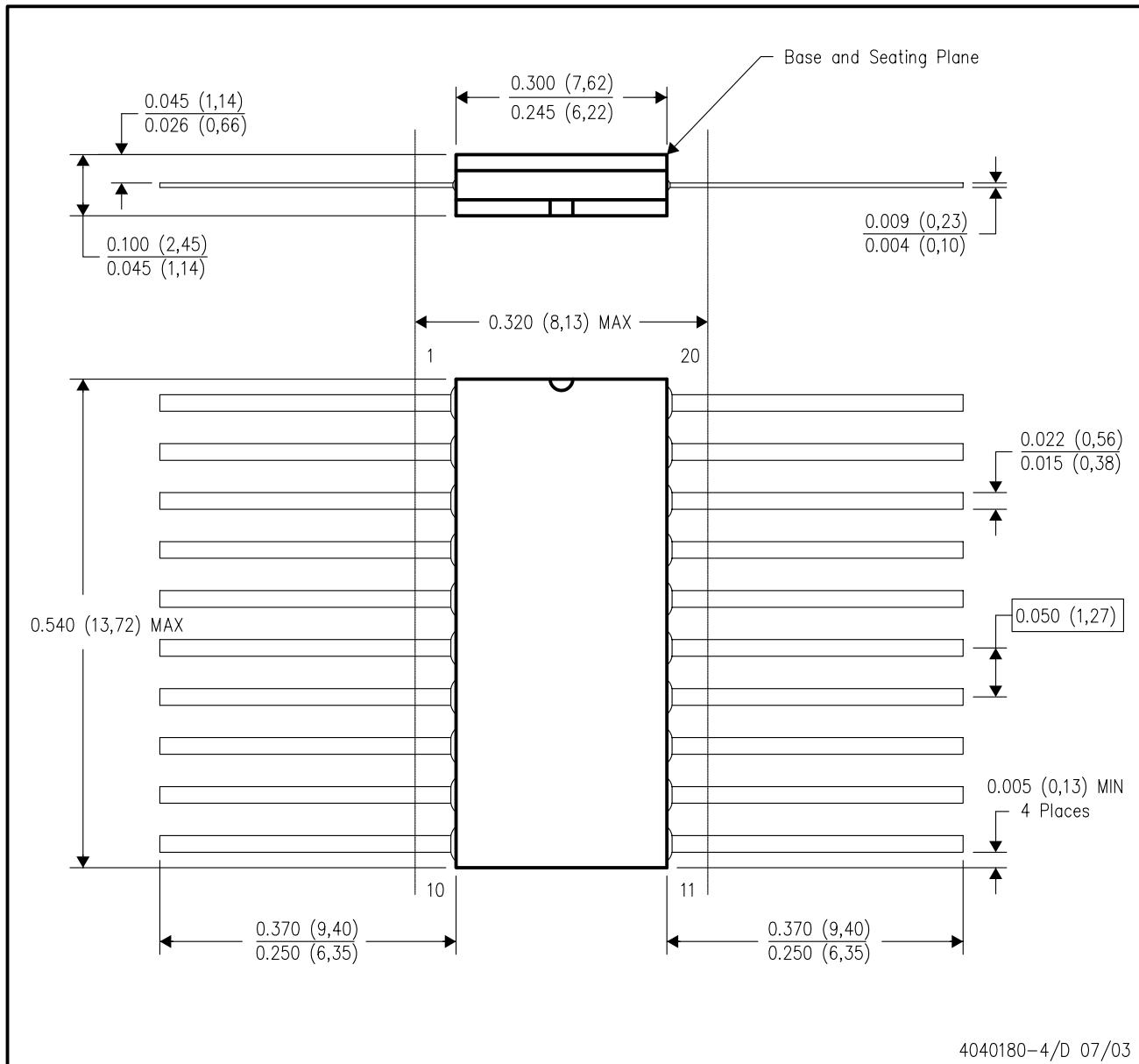


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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



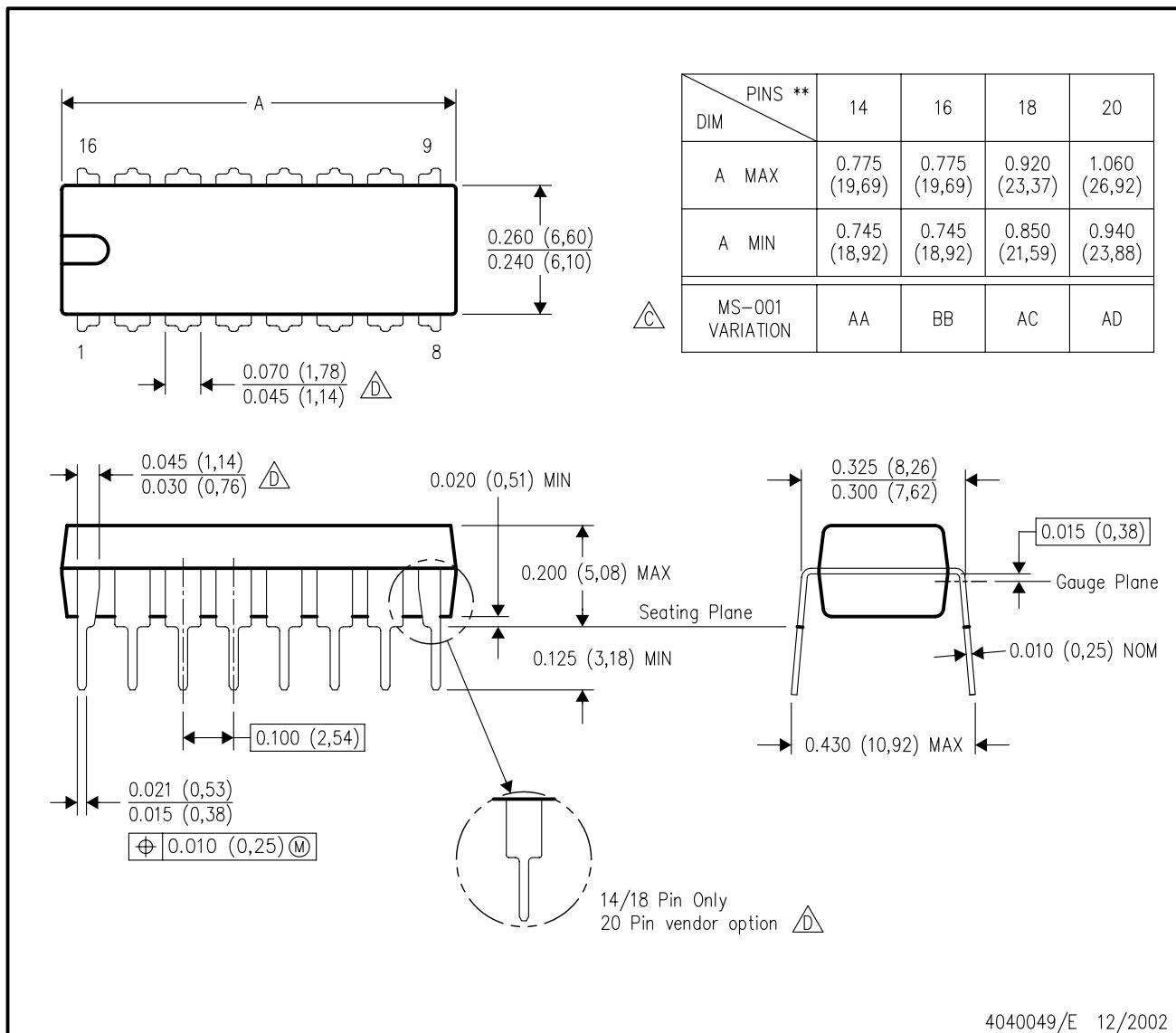
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

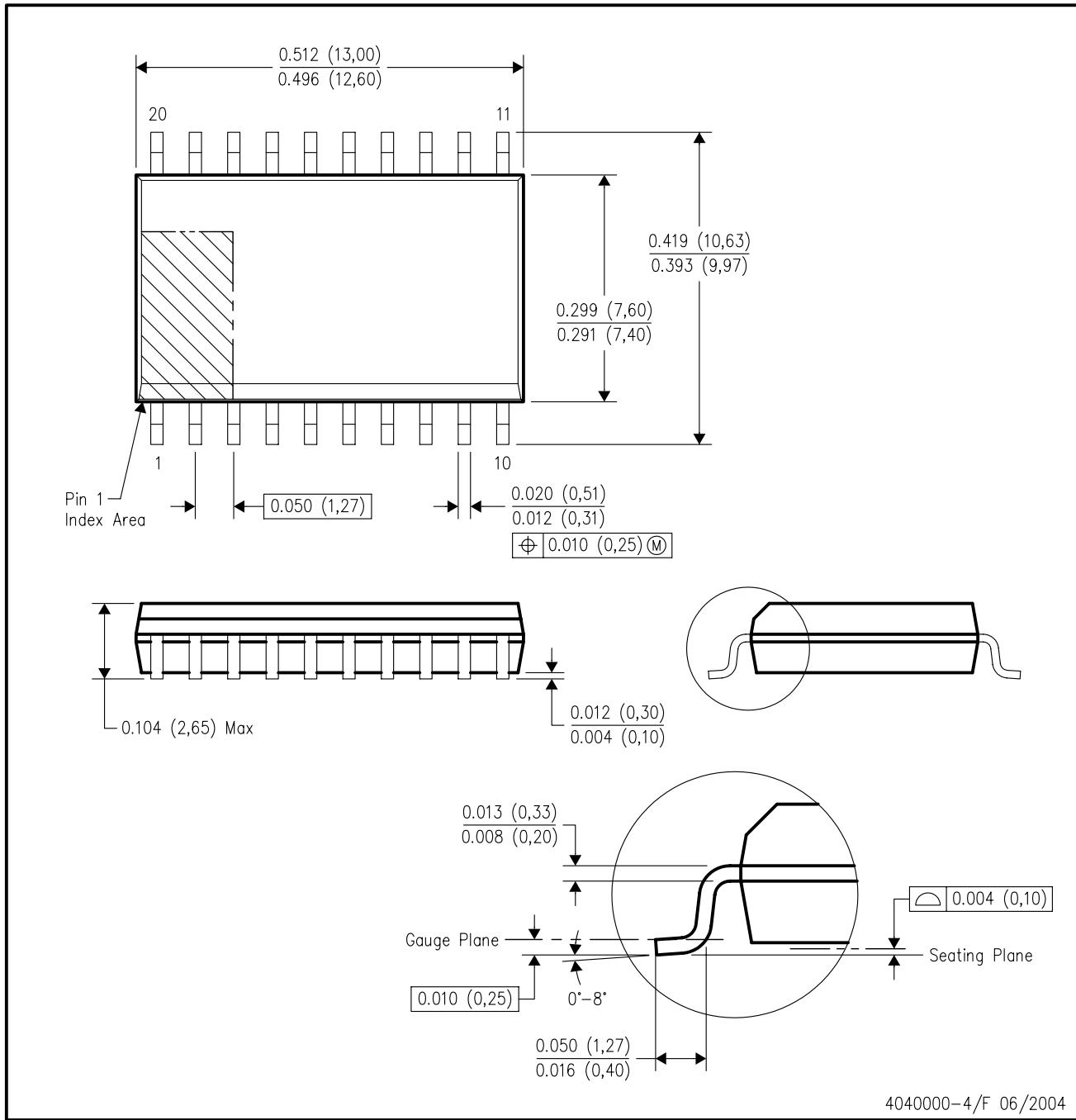
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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