

# TLC193, TLC393 DUAL MICROPOLAR LinCMOS™ VOLTAGE COMPARATOR

SLCS115E – DECEMBER 1986 – REVISED JULY 2003

- **Very Low Power . . . 110  $\mu$ W Typ at 5 V**
- **Fast Response Time . . .  $t_{PLH} = 2.5 \mu$ s Typ**  
With 5-mV Overdrive
- **Single Supply Operation:**
  - TLC393C . . . 3 V to 16 V
  - TLC393I . . . 3 V to 16 V
  - TLC393Q . . . 4 V to 16 V
  - TLC393M . . . 4 V to 16 V
  - TLC193M . . . 4 V to 16 V
- **On-Chip ESD Protection**

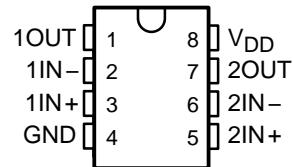
## description

The TLC193 and TLC393 consist of dual independent micropower voltage comparators designed to operate from a single supply. They are functionally similar to the LM393 but uses one-twentieth the power for similar response times. The open-drain MOS output stage interfaces to a variety of loads and supplies. For a similar device with a push-pull output configuration (see the TLC3702 data sheet).

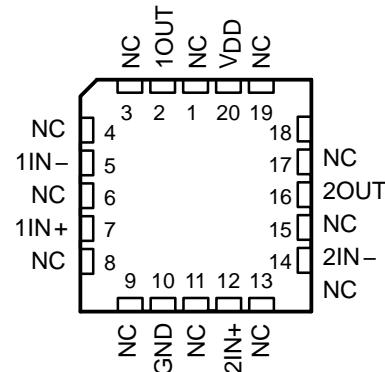
Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC393C is characterized for operation over the commercial temperature range of  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ . The TLC393I is characterized for operation over the extended industrial temperature range of  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ . The TLC393Q is characterized for operation over the full automotive temperature range of  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . The TLC193M and TLC393M are characterized for operation over the full military temperature range of  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ .

**D, JG, P, OR PW PACKAGE  
(TOP VIEW)**

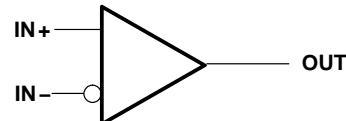


**FK PACKAGE  
(TOP VIEW)**



NC – No internal connection

## symbol (each comparator)



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# **TLC193, TLC393 DUAL MICROPower LinCMOS™ VOLTAGE COMPARATOR**

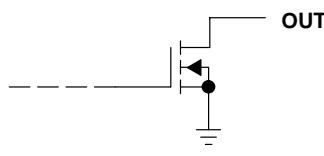
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## AVAILABLE OPTIONS

TA	VI <sub>OMAX</sub> at 25°C	PACKAGES				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	5 mV	TLC393CD	—	—	TLC393CP	TLC393CPWLE
–40°C to 85°C	5 mV	TLC393ID	—	—	TLC393IP	TLC393IPWLE
–40°C to 125°C	5 mV	TLC393QD	—	—	—	—
–55°C to 125°C	5 mV	TLC393MD	TLC193MFK	TLC193MJG	TLC393MP	—

The D package is available tape and reeled. Add the suffix R to the device type (e.g., TLC393CDR).

## **schematic**



### OPEN-DRAIN CMOS OUTPUT

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at IN+ with respect to IN-.

## DISSIPATION RATING TABLE

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—
PW	525 mW	4.2 mW/°C	336 mW	273 mW	—

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**recommended operating conditions**

	TLC393C			UNIT
	MIN	NOM	MAX	
Supply voltage, $V_{DD}$	3	5	16	V
Common-mode input voltage, $V_{IC}$	-0.2		$V_{DD} - 1.5$	V
Low-level output current, $I_{OL}$			20	mA
Operating free-air temperature, $T_A$	0	70		°C

**electrical characteristics at specified operating free-air temperature,  $V_{DD} = 5$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>T</sup>	TA	TLC393C			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = V_{ICR\min}$ , $V_{DD} = 5$ V to 10 V, See Note 3	25°C		1.4	5	mV
		0°C to 70°C			6.5	
$I_{IO}$ Input offset current	$V_{IC} = 2.5$ V	25°C		1		pA
		70°C			0.3	nA
$I_{IB}$ Input bias current	$V_{IC} = 2.5$ V	25°C		5		pA
		70°C			0.6	nA
$V_{ICR}$ Common-mode input voltage range		25°C	0 to $V_{DD} - 1$			V
		0°C to 70°C	0 to $V_{DD} - 1.5$			
CMMR Common-mode rejection ratio	$V_{IC} = V_{ICR\min}$	25°C		84		dB
		70°C		84		
		0°C		84		
$k_{SVR}$ Supply-voltage rejection ratio	$V_{DD} = 5$ V to 10 V	25°C		85		dB
		70°C		85		
		0°C		85		
$V_{OL}$ Low-level output voltage	$V_{ID} = -1$ V, $I_{OL} = 6$ mA	25°C		300	400	mV
		70°C			650	
$I_{OH}$ High-level output current	$V_{ID} = 1$ V, $V_O = 5$ V	25°C		0.8	40	nA
		70°C			1	μA
$I_{DD}$ Supply current (both comparators)	Outputs low, No load	25°C		22	40	μA
		0°C to 70°C			50	

<sup>T</sup> All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

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## recommended operating conditions

	TLC393I			UNIT
	MIN	NOM	MAX	
Supply voltage, $V_{DD}$	3	5	16	V
Common-mode input voltage, $V_{IC}$	-0.2		$V_{DD} - 1.5$	V
Low-level output current, $I_{OL}$			20	mA
Operating free-air temperature, $T_A$	-40		85	°C

## electrical characteristics at specified operating free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	$T_A$	TLC393I			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = V_{ICR\min}$ , $V_{DD} = 5$ V to 10 V, See Note 3	25°C		1.4	5	mV
		-40°C to 85°C			7	
$I_{IO}$ Input offset current	$V_{IC} = 2.5$ V	25°C		1	pA	pA
		85°C			1	
$I_{IB}$ Input bias current	$V_{IC} = 2.5$ V	25°C		5	pA	nA
		85°C			2	
$V_{ICR}$ Common-mode input voltage range		25°C	0 to $V_{DD} - 1$			V
		-40°C to 85°C	0 to $V_{DD} - 1.5$			
CMMR Common-mode rejection ratio	$V_{IC} = V_{ICR\min}$	25°C		84		dB
		85°C		84		
		-40°C		84		
$k_{SVR}$ Supply-voltage rejection ratio	$V_{DD} = 5$ V to 10 V	25°C		85		dB
		85°C		85		
		-40°C		84		
$V_{OL}$ Low-level output voltage	$V_{ID} = -1$ V, $I_{OL} = 6$ mA	25°C		300	400	mV
		85°C			700	
$I_{OH}$ High-level output current	$V_{ID} = 1$ V, $V_O = 5$ V	25°C		0.8	40	nA
		85°C			1	
$I_{DD}$ Supply current (both comparators)	Outputs low, No load	25°C		22	40	$\mu$ A
		-40°C to 85°C			65	

<sup>†</sup> All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

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**recommended operating conditions**

	TLC393Q			UNIT
	MIN	NOM	MAX	
Supply voltage, $V_{DD}$	4	5	16	V
Common-mode input voltage, $V_{IC}$	0	$V_{DD} - 1.5$		V
Low-level output current, $I_{OL}$		20		mA
Operating free-air temperature, $T_A$	-40	125		°C

**electrical characteristics at specified operating free-air temperature,  $V_{DD} = 5$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	$T_A$	TLC393Q			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = V_{ICR\min}$ , $V_{DD} = 5$ V to 10 V, See Note 4	25°C		1.4	5	mV
		-40°C to 125°C			10	
$I_{IO}$ Input offset current	$V_{IC} = 2.5$ V	25°C		1		pA
		125°C			15	nA
$I_{IB}$ Input bias current	$V_{IC} = 2.5$ V	25°C		5		pA
		125°C			30	nA
$V_{ICR}$ Common-mode input voltage range		25°C	0 to $V_{DD} - 1$			V
		-40°C to 125°C	0 to $V_{DD} - 1.5$			
CMMR Common-mode rejection ratio	$V_{IC} = V_{ICR\min}$	25°C		84		dB
		125°C		84		
		-40°C		84		
$k_{SVR}$ Supply-voltage rejection ratio	$V_{DD} = 5$ V to 10 V	25°C		85		dB
		125°C		84		
		-40°C		84		
$V_{OL}$ Low-level output voltage	$V_{ID} = -1$ V, $I_{OL} = 6$ mA	25°C		300	400	mV
		125°C			800	
$I_{OH}$ High-level output current	$V_{ID} = 1$ V, $V_O = 5$ V	25°C		0.8	40	nA
		125°C			1	μA
$I_{DD}$ Supply current (both comparators)	Outputs low, No load	25°C		22	40	μA
		-40°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V (with a 2.5-kΩ load to  $V_{DD}$ ).

# TLC193, TLC393 DUAL MICROPOWER LinCMOS™ VOLTAGE COMPARATOR

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## recommended operating conditions

	TLC193M, TLC393M			UNIT
	MIN	NOM	MAX	
Supply voltage, $V_{DD}$	4	5	16	V
Common-mode input voltage, $V_{IC}$	0		$V_{DD} - 1.5$	V
Low-level output current, $I_{OL}$			20	mA
Operating free-air temperature, $T_A$	-55		125	°C

## electrical characteristics at specified operating free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	$T_A$	TLC193M, TLC393M			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = V_{ICR\min}$ , $V_{DD} = 5$ V to 10 V, See Note 4	25°C		1.4	5	mV
		-55°C to 125°C			10	
$I_{IO}$ Input offset current	$V_{IC} = 2.5$ V	25°C		1		pA
		125°C			15	nA
$I_{IB}$ Input bias current	$V_{IC} = 2.5$ V	25°C		5		pA
		125°C			30	nA
$V_{ICR}$ Common-mode input voltage range		25°C	0 to $V_{DD} - 1$			V
		-55°C to 125°C	0 to $V_{DD} - 1.5$			
CMMR Common-mode rejection ratio	$V_{IC} = V_{ICR\min}$	25°C		84		dB
		125°C		84		
		-55°C		84		
$k_{SVR}$ Supply-voltage rejection ratio	$V_{DD} = 5$ V to 10 V	25°C		85		dB
		125°C		84		
		-55°C		84		
$V_{OL}$ Low-level output voltage	$V_{ID} = -1$ V, $I_{OL} = 6$ mA	25°C		300	400	mV
		125°C			800	
$I_{OH}$ High-level output current	$V_{ID} = 1$ V, $V_O = 5$ V	25°C		0.8	40	nA
		125°C			1	μA
$I_{DD}$ Supply current (both comparators)	Outputs low, No load	25°C		22	40	μA
		-55°C to 125°C			90	

<sup>†</sup> All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V (with a 2.5-kΩ load to  $V_{DD}$ ).

switching characteristics,  $V_{DD} = 5$  V,  $T_A = 25^\circ\text{C}$  (see Figure 3)

PARAMETER	TEST CONDITIONS	TLC393C, TLC393I TLC393Q, TLC193M, TLC393M			UNIT
		MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	$f = 10$ kHz, $C_L = 15$ pF	Overdrive = 2 mV	4.5		$\mu\text{s}$
		Overdrive = 5 mV	2.5		
		Overdrive = 10 mV	1.7		
		Overdrive = 20 mV	1.2		
		Overdrive = 40 mV	1.1		
$t_{PHL}$ Propagation delay time, high-to-low-level output	$f = 10$ kHz, $C_L = 15$ pF	$V_I = 1.4$ -V step at IN+	1.1		$\mu\text{s}$
		Overdrive = 2 mV	3.6		
		Overdrive = 5 mV	2.1		
		Overdrive = 10 mV	1.3		
		Overdrive = 20 mV	0.85		
		Overdrive = 40 mV	0.55		
$t_f$ Fall time, output	$f = 10$ kHz, $C_L = 15$ pF	$V_I = 1.4$ -V step at IN+	0.10		ns
		Overdrive = 50 mV	22		

### PARAMETER MEASUREMENT INFORMATION

The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection ratio, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the  $V_{ICR}$  test, rather than changing the input voltages, to provide greater accuracy.

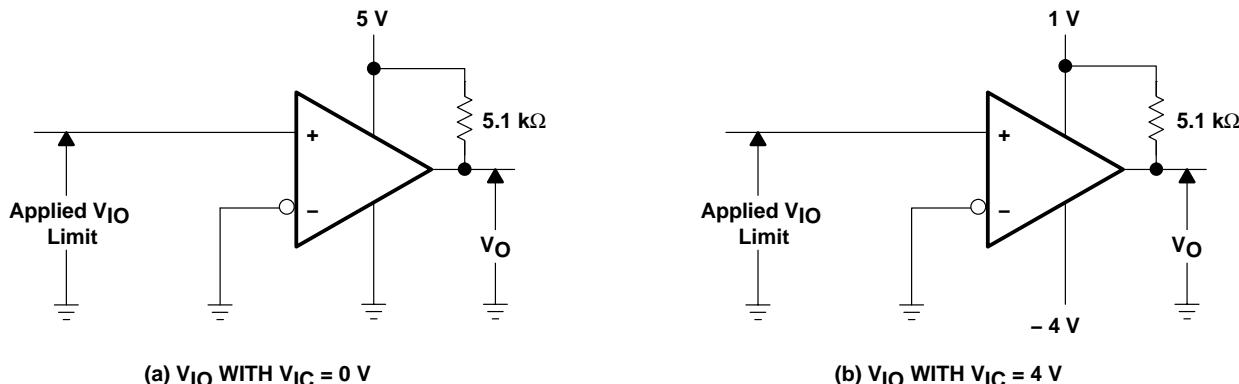


Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

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## PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

The voltage divider formed by R9 and R10 provides an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

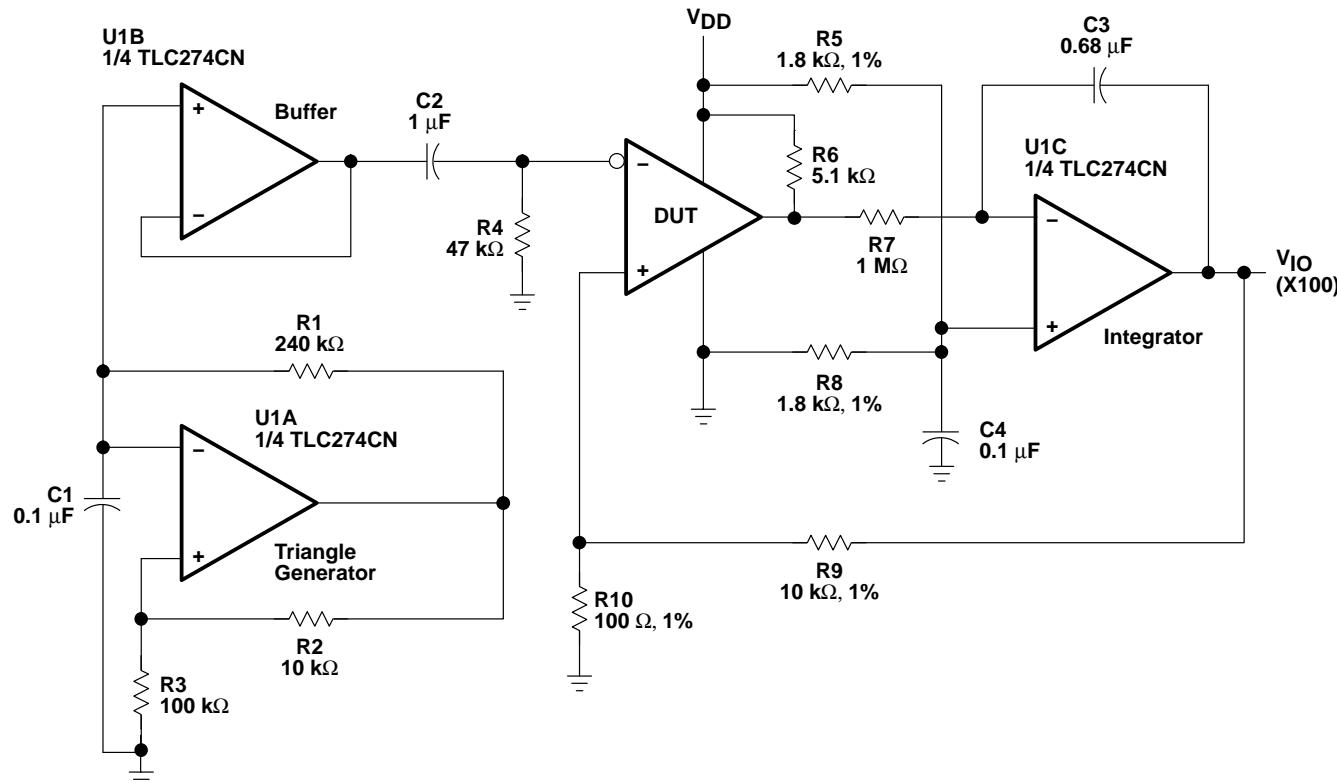
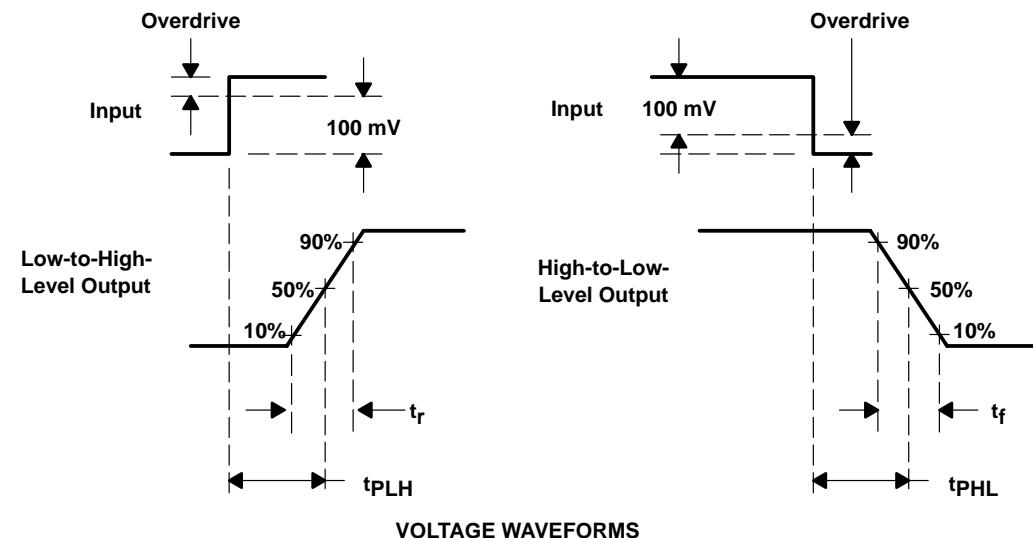
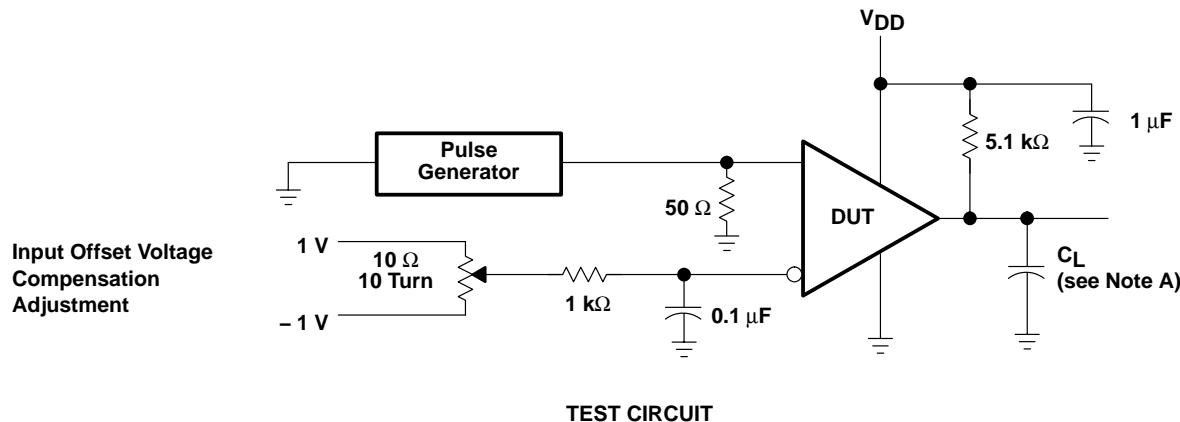


Figure 2. Circuit for Input Offset Voltage Measurement

### PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example, 105 mV or 5 mV overdrive, causes the output to change state.



NOTE A:  $C_L$  includes probe and jig capacitance.

**Figure 3. Propagation Delay, Rise Time, and Fall Time Circuit and Voltage Waveforms**

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## TYPICAL CHARACTERISTICS

Table of Graphs

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$I_{IB}$	Input bias current	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Free-air temperature	6
$k_{SVR}$	Supply-voltage rejection ratio	vs Free-air temperature	7
$V_{OL}$	Low-level output voltage	vs Low-level output current	8
		vs Free-air temperature	9
$I_{OH}$	Low-level output current	vs High-level output voltage	10
		vs Free-air temperature	11
$I_{DD}$	Supply current	vs Supply voltage	12
		vs Free-air temperature	13
$t_{PLH}$	Low-to-high level output propagation delay time	vs Supply voltage	14
$t_{PHL}$	High-to-low level output propagation delay time	vs Supply voltage	15
	Low-to-high-level output response	Low-to-high level output propagation delay time	16
	High-to-low level output response	High-to-low level output propagation delay time	17
$t_f$	Fall time	vs Supply voltage	18

DISTRIBUTION OF INPUT OFFSET VOLTAGE†

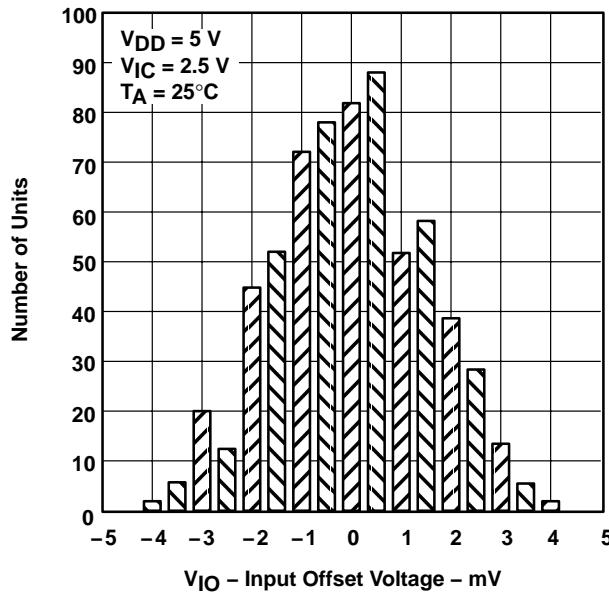


Figure 4

INPUT BIAS CURRENT  
vs  
FREE-AIR TEMPERATURE†

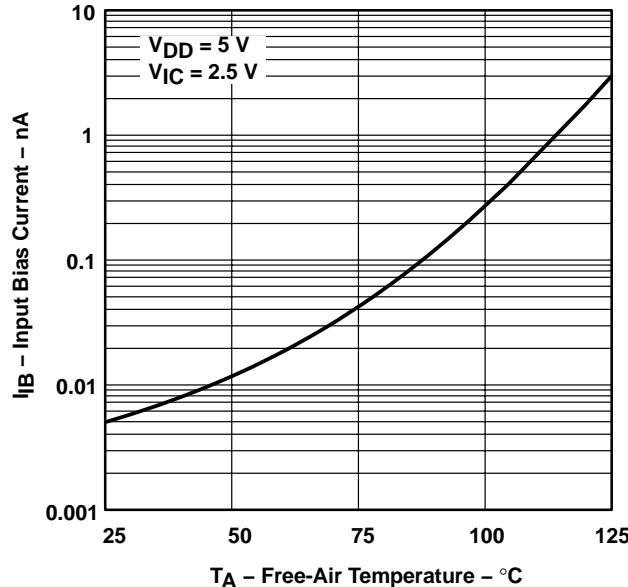


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



**TYPICAL CHARACTERISTICS<sup>†</sup>**

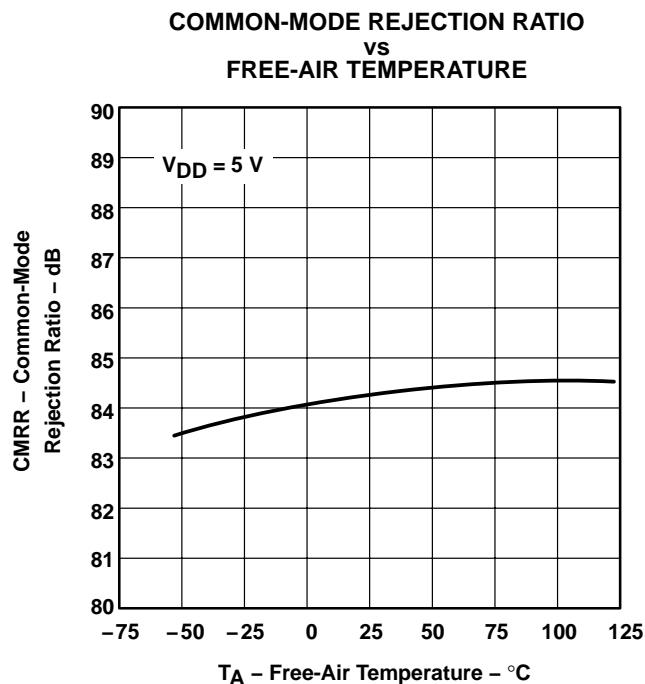


Figure 6

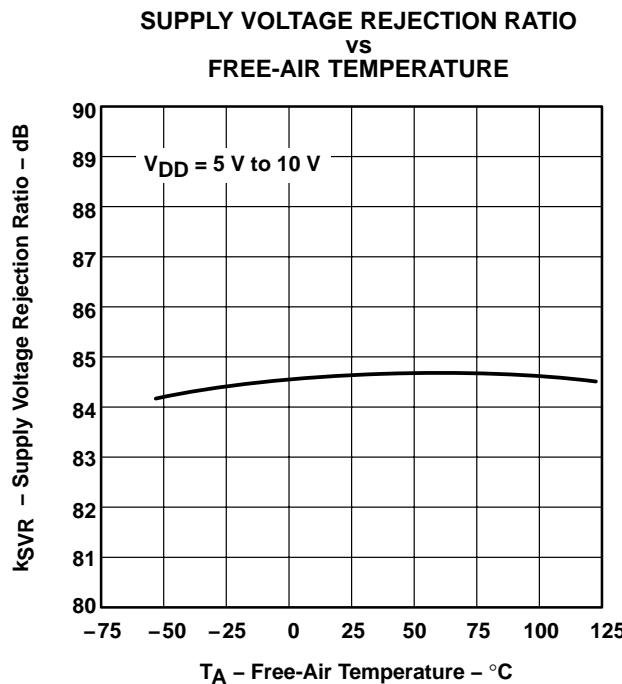


Figure 7

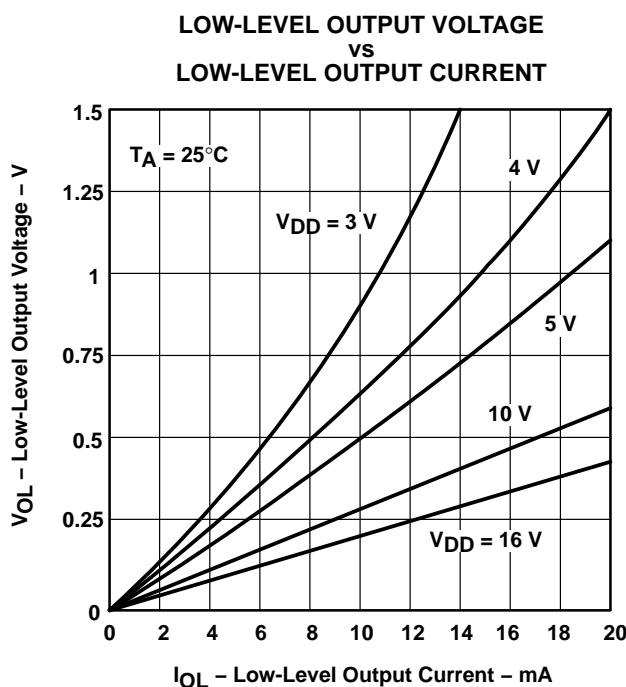


Figure 8

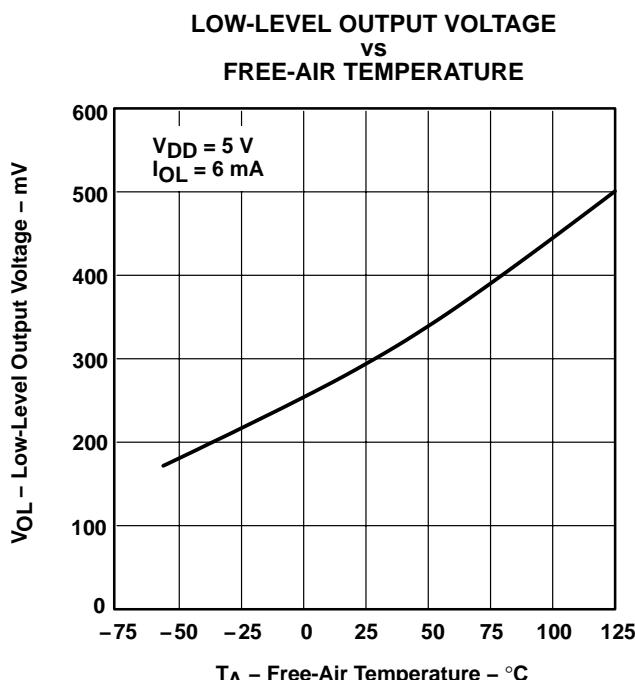


Figure 9

<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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## TYPICAL CHARACTERISTICS†

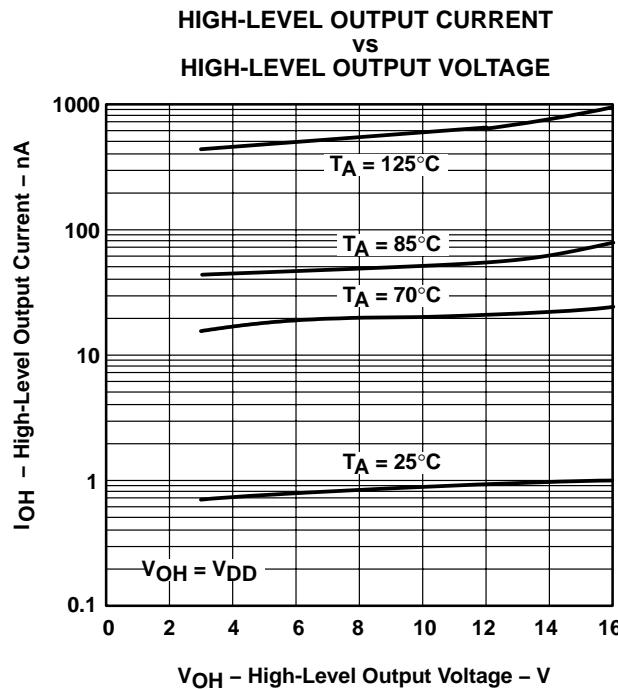


Figure 10

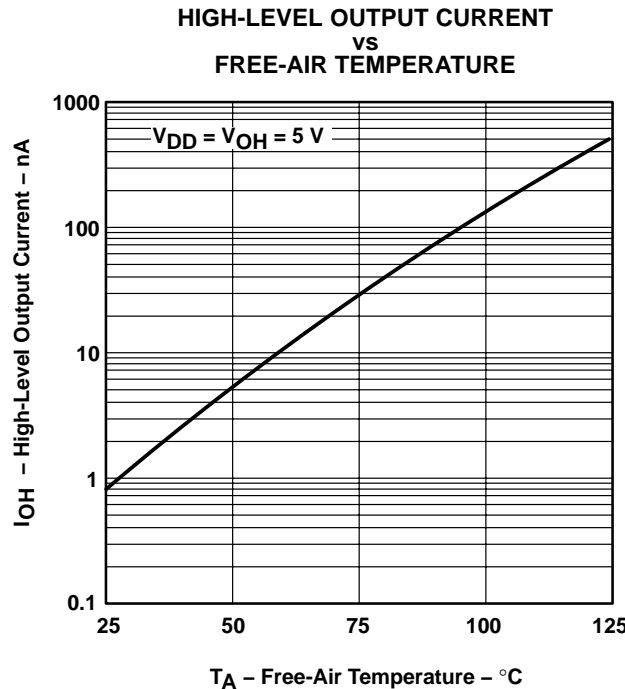


Figure 11

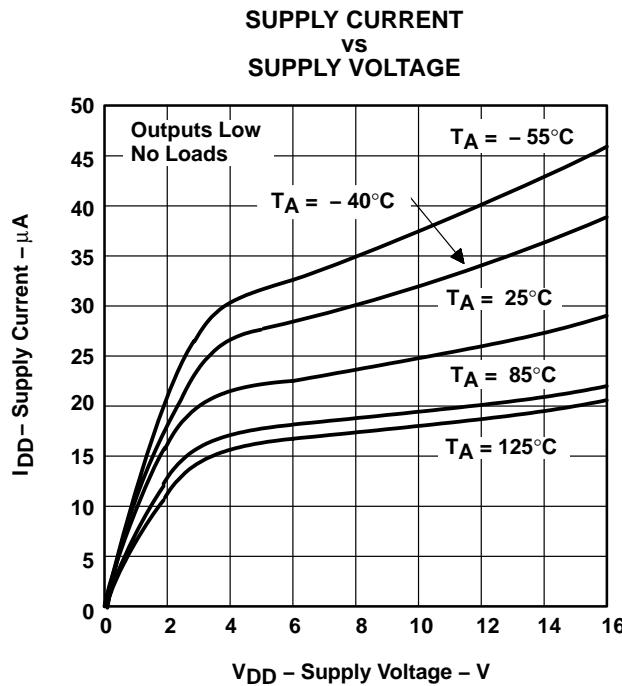


Figure 12

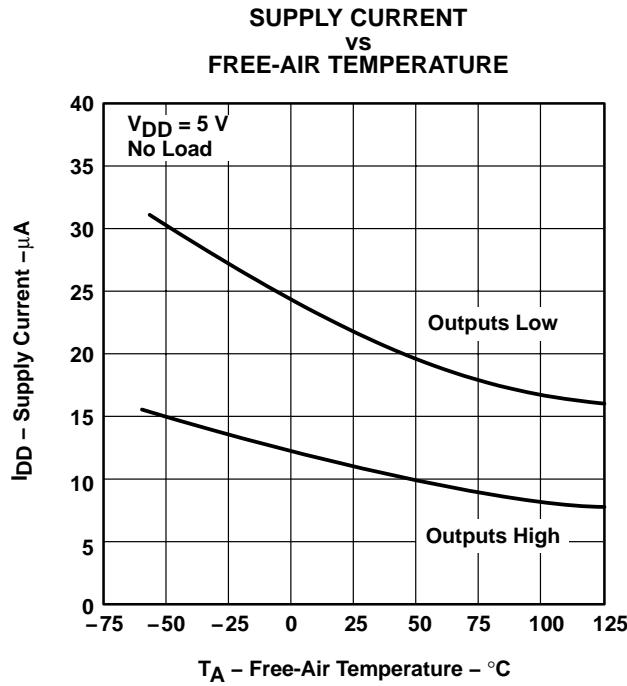
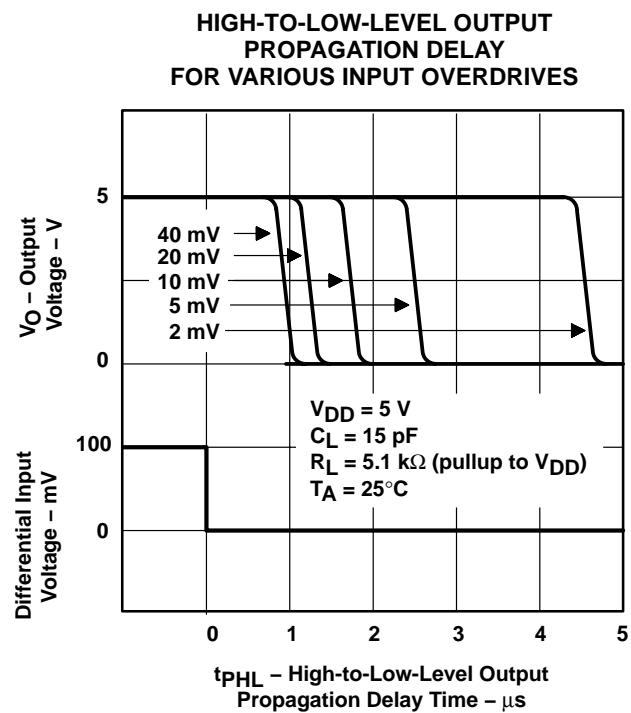
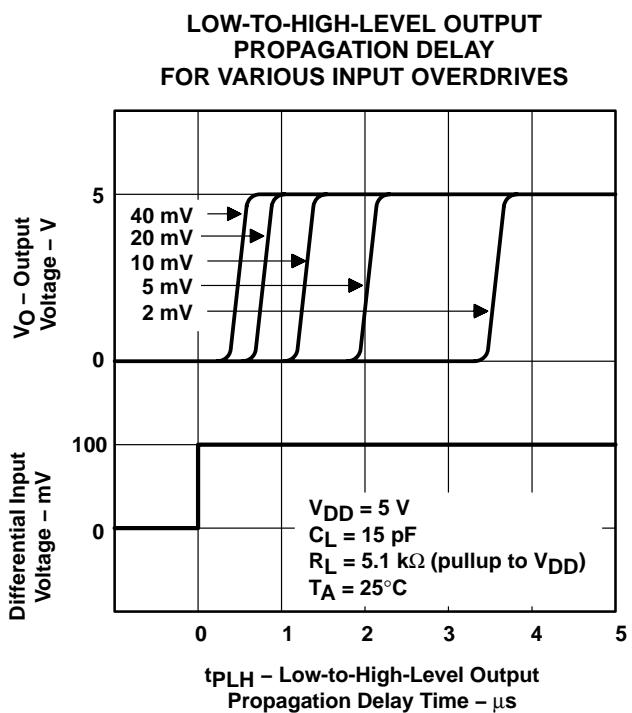
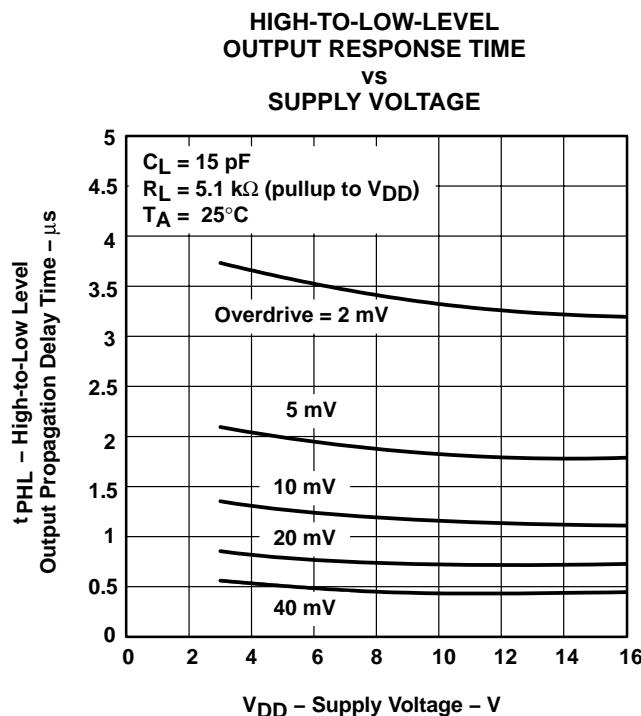
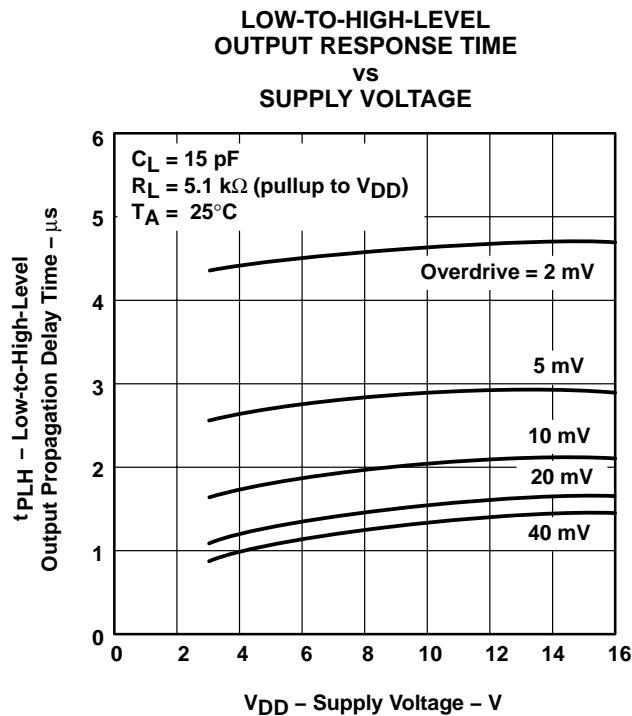


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TYPICAL CHARACTERISTICS**



# TLC193, TLC393 DUAL MICROPOWER LinCMOS™ VOLTAGE COMPARATOR

SLCS115D – DECEMBER 1986 – REVISED JULY 2003

## TYPICAL CHARACTERISTICS

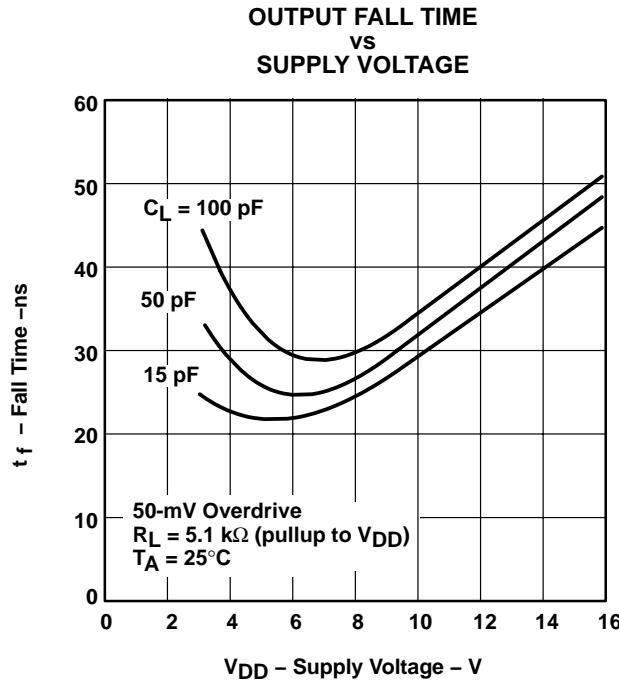


Figure 18

## APPLICATION INFORMATION

The input should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with  $V_{DD} = 5$  V, both inputs must remain between –0.2 V and 4 V to assure proper device operation.

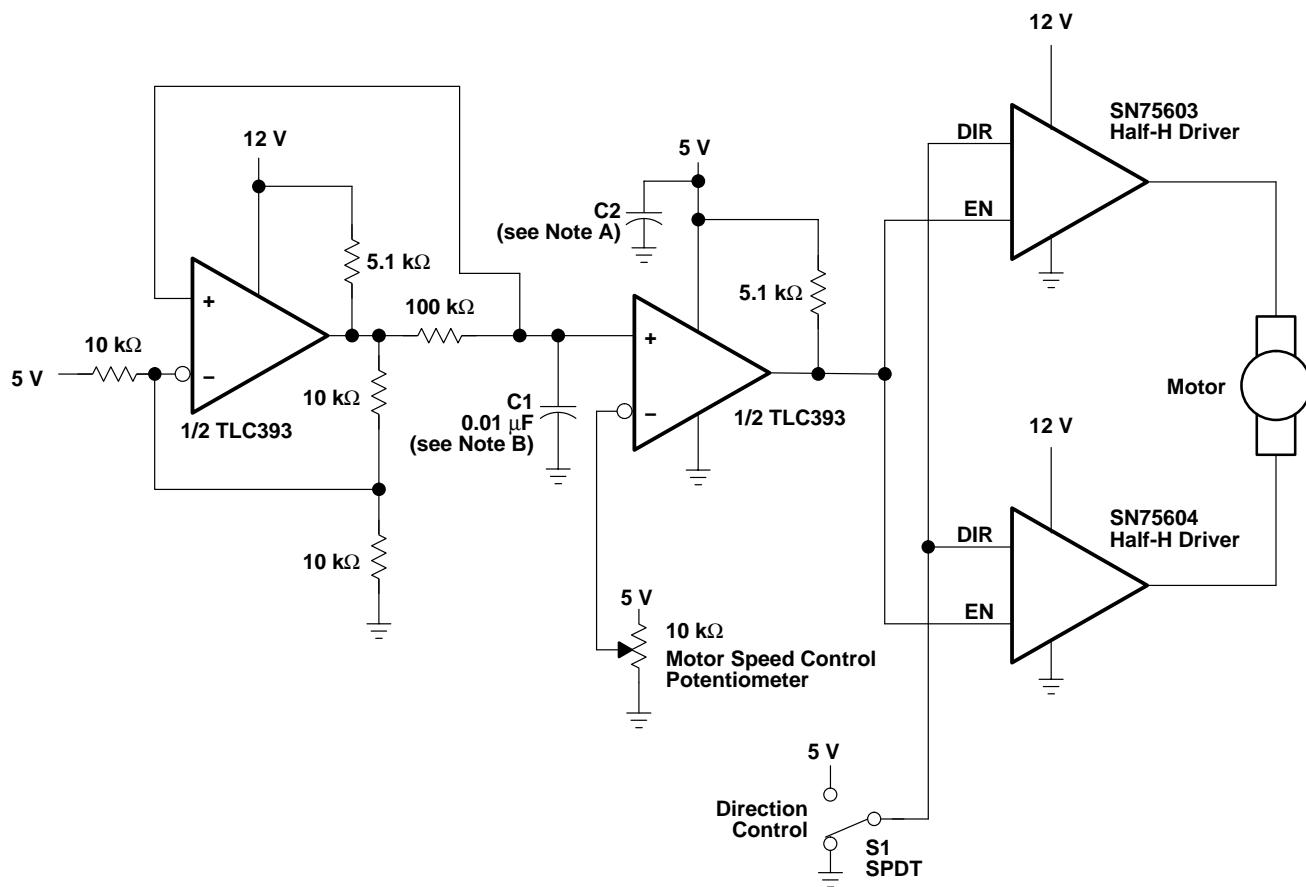
To assure reliable operation, the supply should be decoupled with a capacitor (0.1- $\mu\text{F}$ ) positioned as close to the device as possible.

The TLC393 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

	FIGURE
Pulse-width-modulated motor speed controller	19
Enhanced supply supervisor	20
Two-phase nonoverlapping clock generator	21
Micropower switching regulator	28

**APPLICATION INFORMATION**



NOTES: A. The recommended minimum capacitance is 10  $\mu$ F to eliminate common ground switching noise.  
 B. Adjust C1 for change in oscillator frequency.

**Figure 19. Pulse-Width-Modulated Motor Speed Controller**

# TLC193, TLC393 DUAL MICROPOWER LinCMOS™ VOLTAGE COMPARATOR

SLCS115D – DECEMBER 1986 – REVISED JULY 2003

## APPLICATION INFORMATION

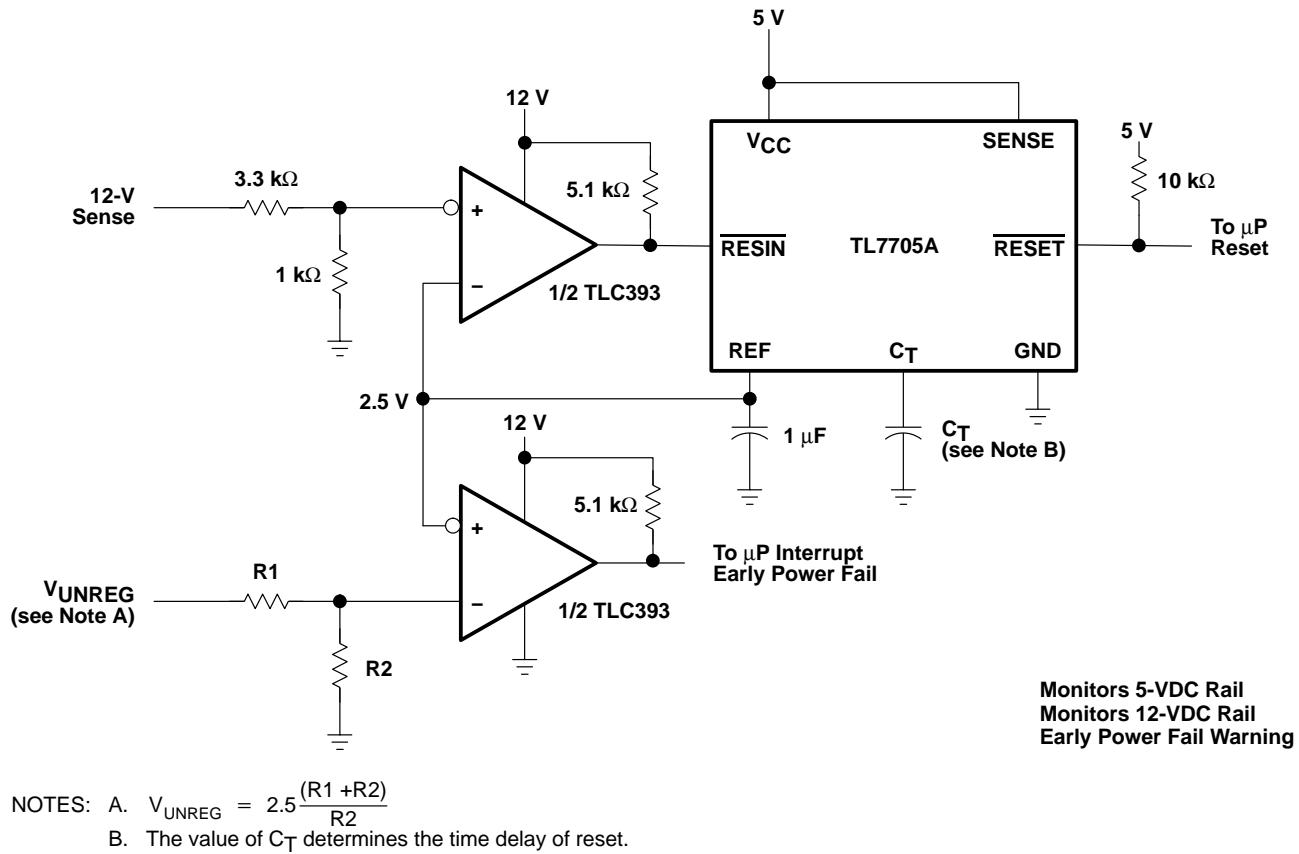
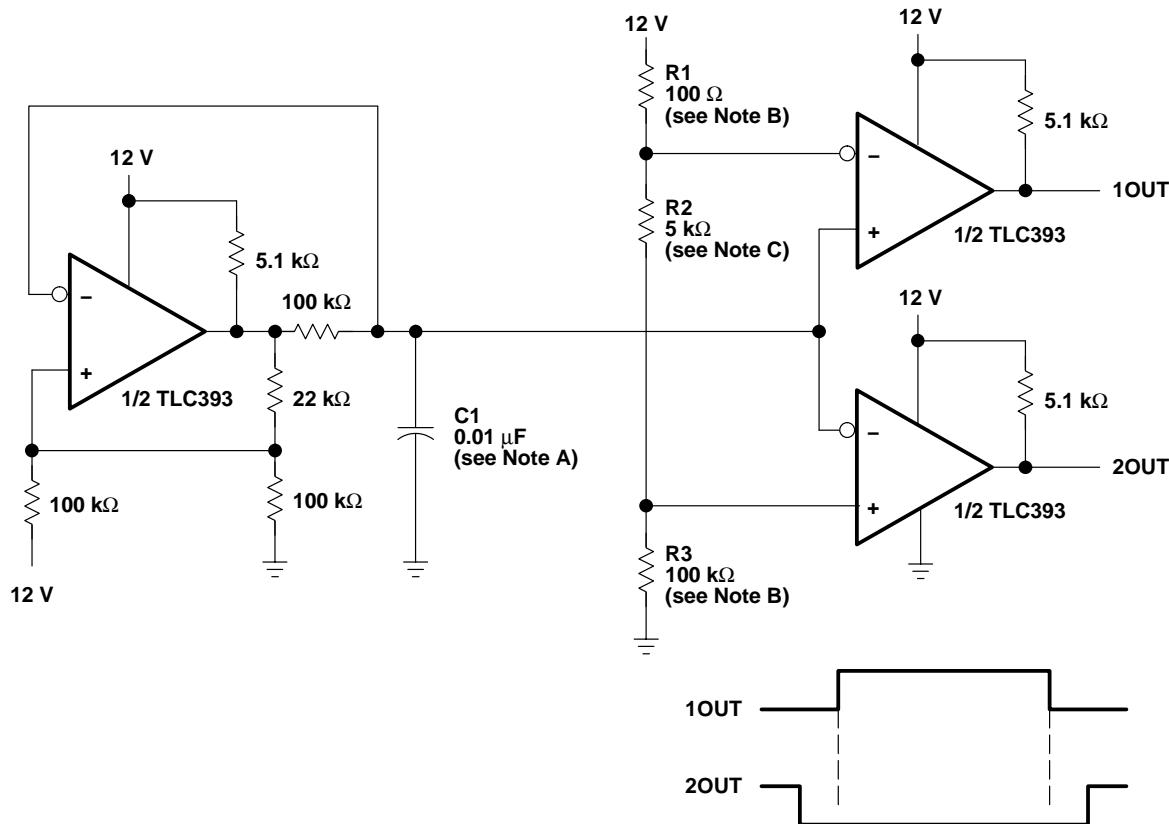


Figure 20. Enhanced Supply Supervisor

**APPLICATION INFORMATION**



NOTES: A. Adjust C1 for a change in oscillator frequency where:

$$1/f = 1.85(100 \text{ k}\Omega)C1$$

B. Adjust R1 and R3 to change duty cycle

C. Adjust R2 to change deadtime

**Figure 21. Two-Phase Nonoverlapping Clock Generator**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9555101NXDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
5962-9555101QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC193MFKB	OBsolete	LCCC	FK	20		TBD	Call TI	Call TI
TLC193MJG	OBsolete	CDIP	JG	8		TBD	Call TI	Call TI
TLC193MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC393CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC393CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC393CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC393CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC393CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC393CPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/Level-1-220C-UNLIM
TLC393CPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC393CPWLE	OBsolete	TSSOP	PW	8		TBD	Call TI	Call TI
TLC393CPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC393CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC393ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC393IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC393IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC393IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC393IPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC393IPWLE	OBsolete	TSSOP	PW	8		TBD	Call TI	Call TI
TLC393IPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC393MD	OBsolete	SOIC	D	8		TBD	Call TI	Call TI
TLC393MP	OBsolete	PDIP	P	8		TBD	Call TI	Call TI
TLC393QDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

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for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

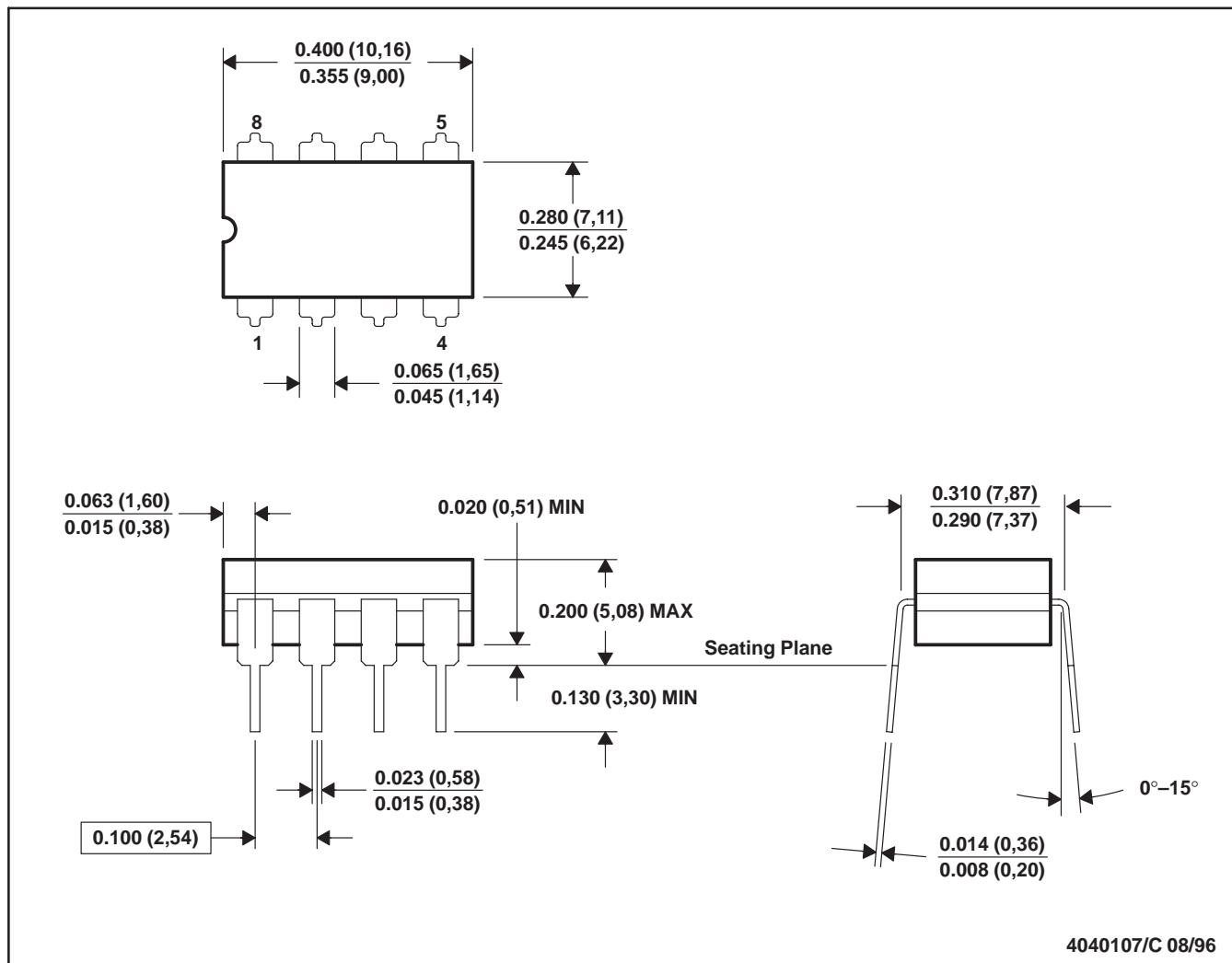
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

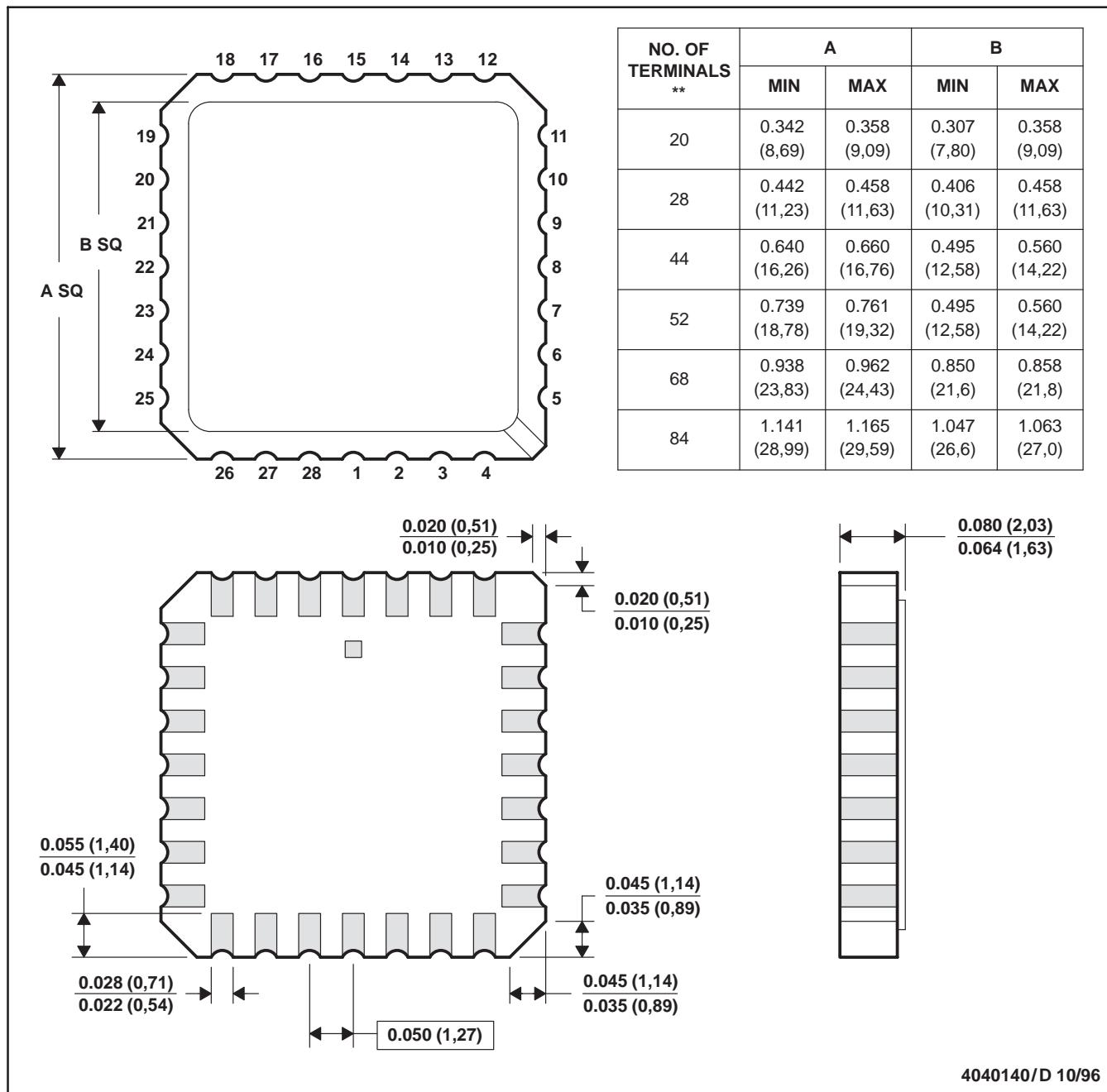


NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

## 28 TERMINAL SHOWN

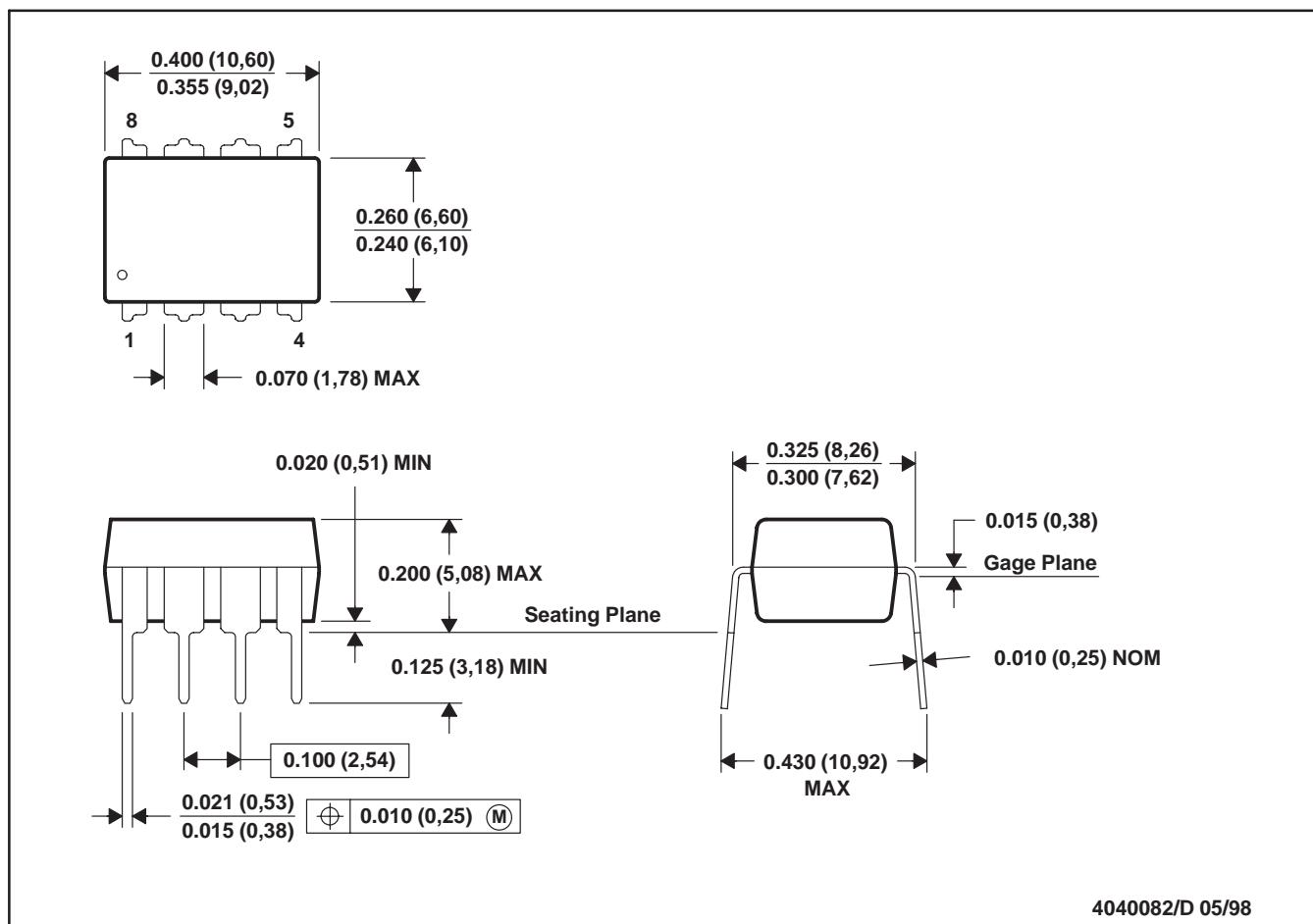


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE

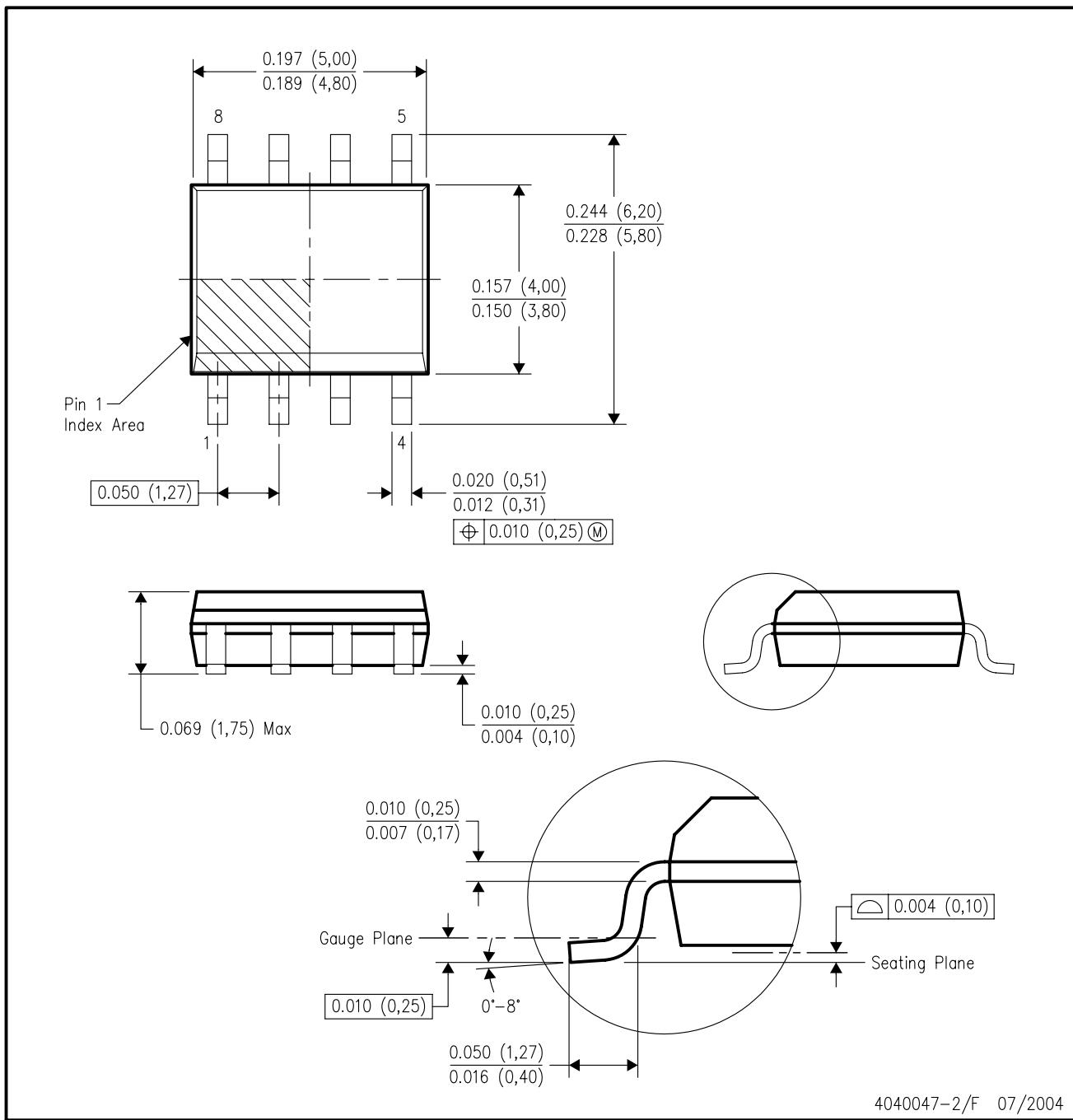


NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

## D (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-2/F 07/2004

NOTES:

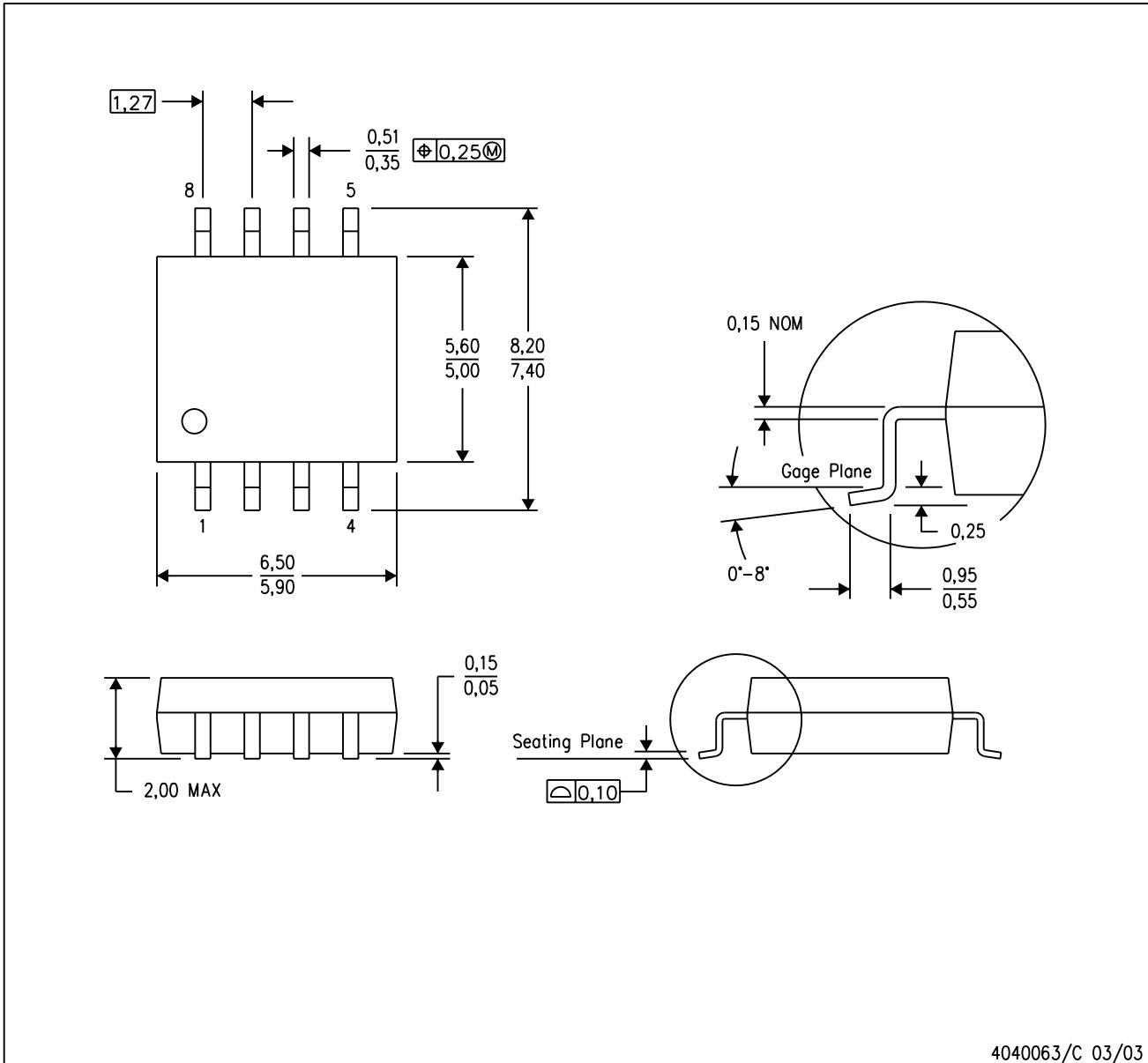
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-012 variation AA.

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## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



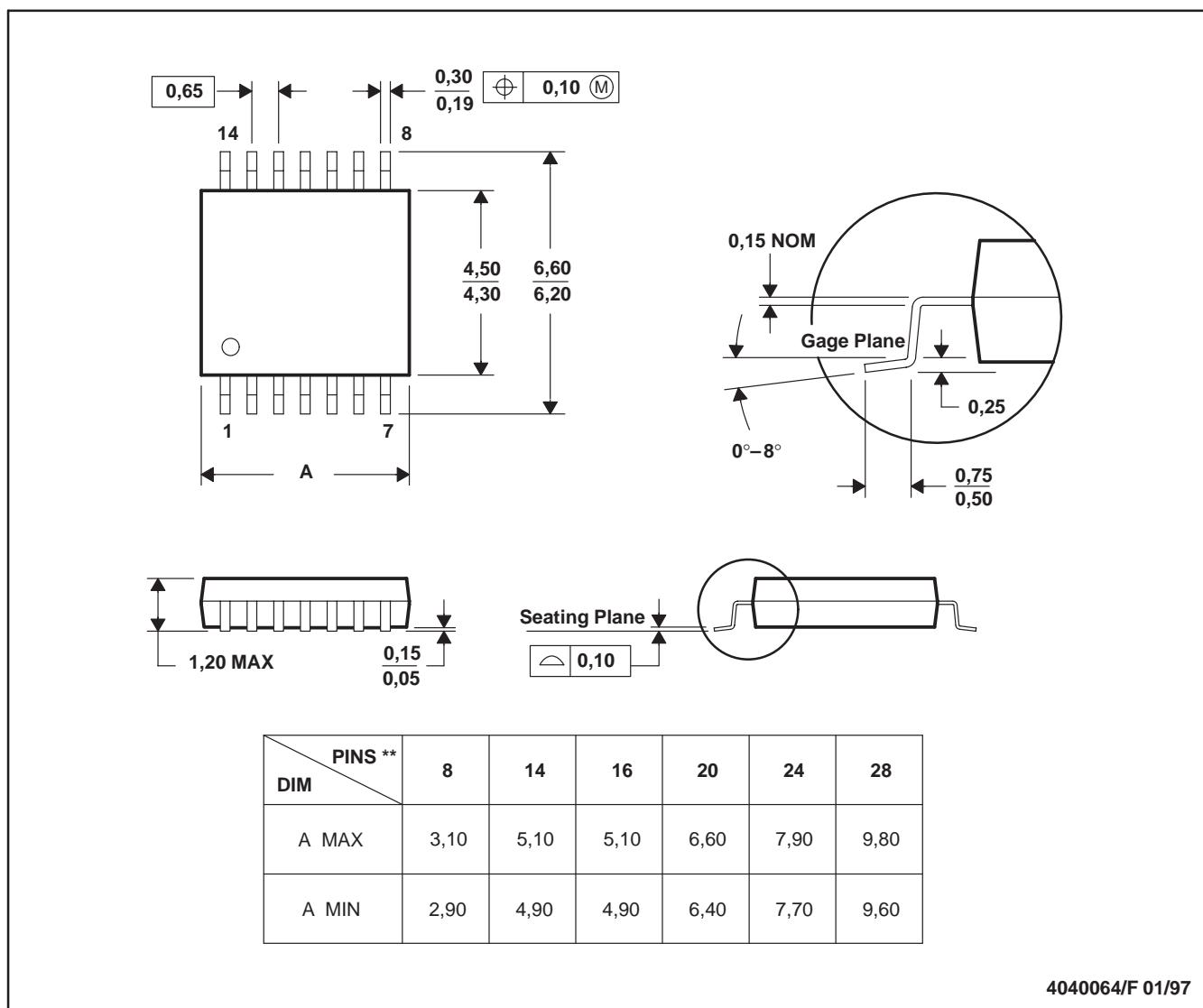
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

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