

RELIABILITY REPORT
FOR
MAX813LxxA
PLASTIC ENCAPSULATED DEVICES

June 5, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX813L successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX813L microprocessor(μ P) supervisory circuit reduces the complexity and number of components required to monitor power-supply and battery functions in μ P systems. This device significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The MAX813L provides four functions:

- 1) A reset output during power-up, power-down, and brownout conditions.
- 2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds.
- 3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
- 4) An active-low manual-reset input.

This device provides RESET instead of /RESET. The MAX813L generates a reset pulse when the supply voltage drops below 4.65V.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
All Other Inputs (Note 1)	-0.3V to (V_{CC} + 0.3V)
Input Current	
V_{CC}	20mA
GND	20mA
Output Current (all outputs)	20mA
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	471mW
Derates above +70°C	5.88mW/°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin SO	471mW
8-Pin PDIP	727mW
8-Pin uMAX	330mW
Derates above +70°C	5.88mW/°C
8-Pin SO	9.09mW/°C
8-Pin PDIP	4.10.mW/°C

Note 1: The input voltage limits on PFI and /MR can be exceeded if the input current is less than 10mA.

II. Manufacturing Information

A. Description/Function:	Low-Cost, μ P Supervisory Circuit
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	572
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	December, 1995

III. Packaging Information

A. Package Type:	8-Lead SO	8-Lead PDIP	8-Lead uMAX
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1701-0101	# 05-1701-0100	# 05-1701-0164
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	51x74 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts:
 - Jim Pedicord (Manager, Reliability Operations)
 - Bryan Preeshl (Executive Director)
 - Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 2480 \times 2}$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 0.97 \times 10^{-9}$$

$$\lambda = 0.97 \text{ F.I.T. (60% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5035) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PW27-11 die type has been found to have all pins able to withstand a transient pulse of $\pm 1500V$ per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 100mA$.

Table 1
Reliability Evaluation Test Results

MAX813LxxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		2480	1
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO PDIP uMAX	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

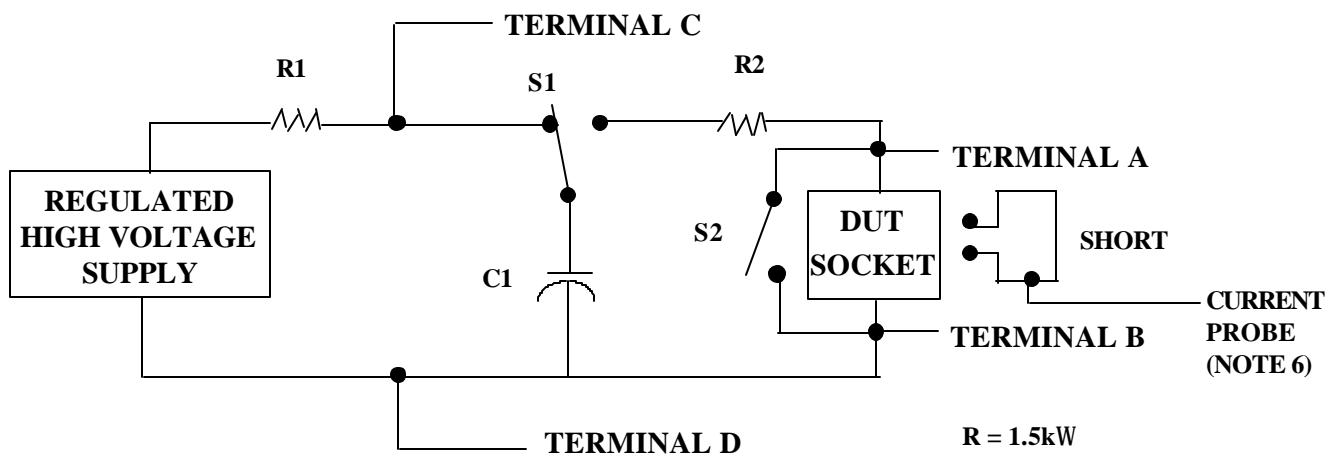
1/ Table II is restated in narrative form in 3.4 below.

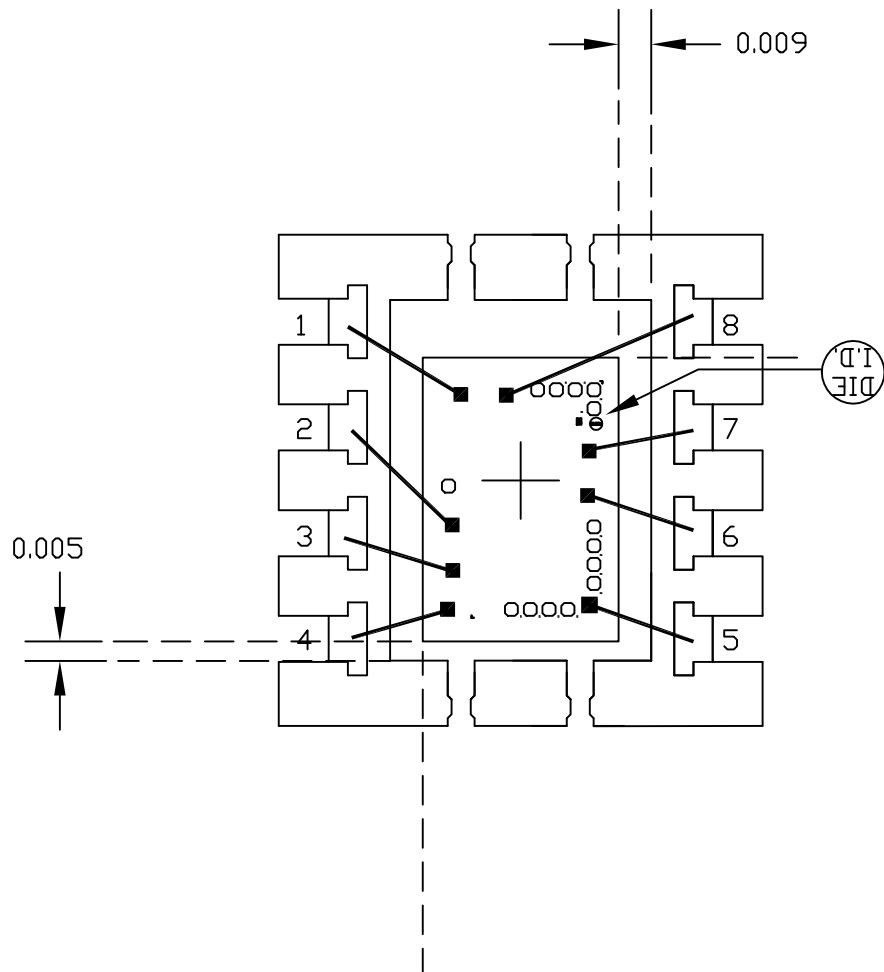
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

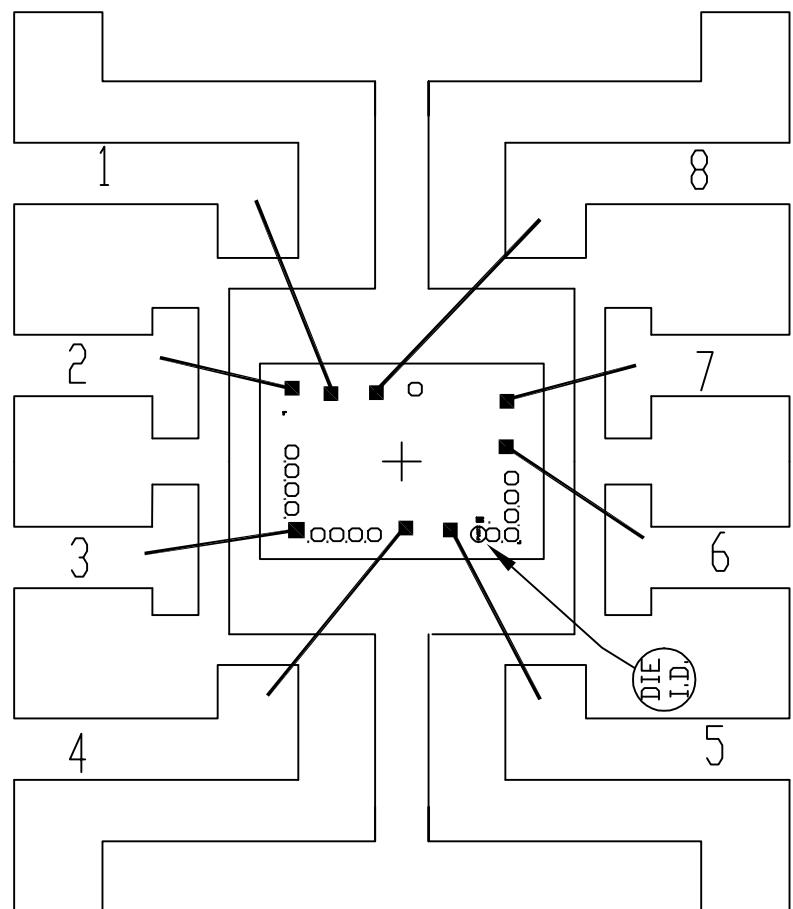
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

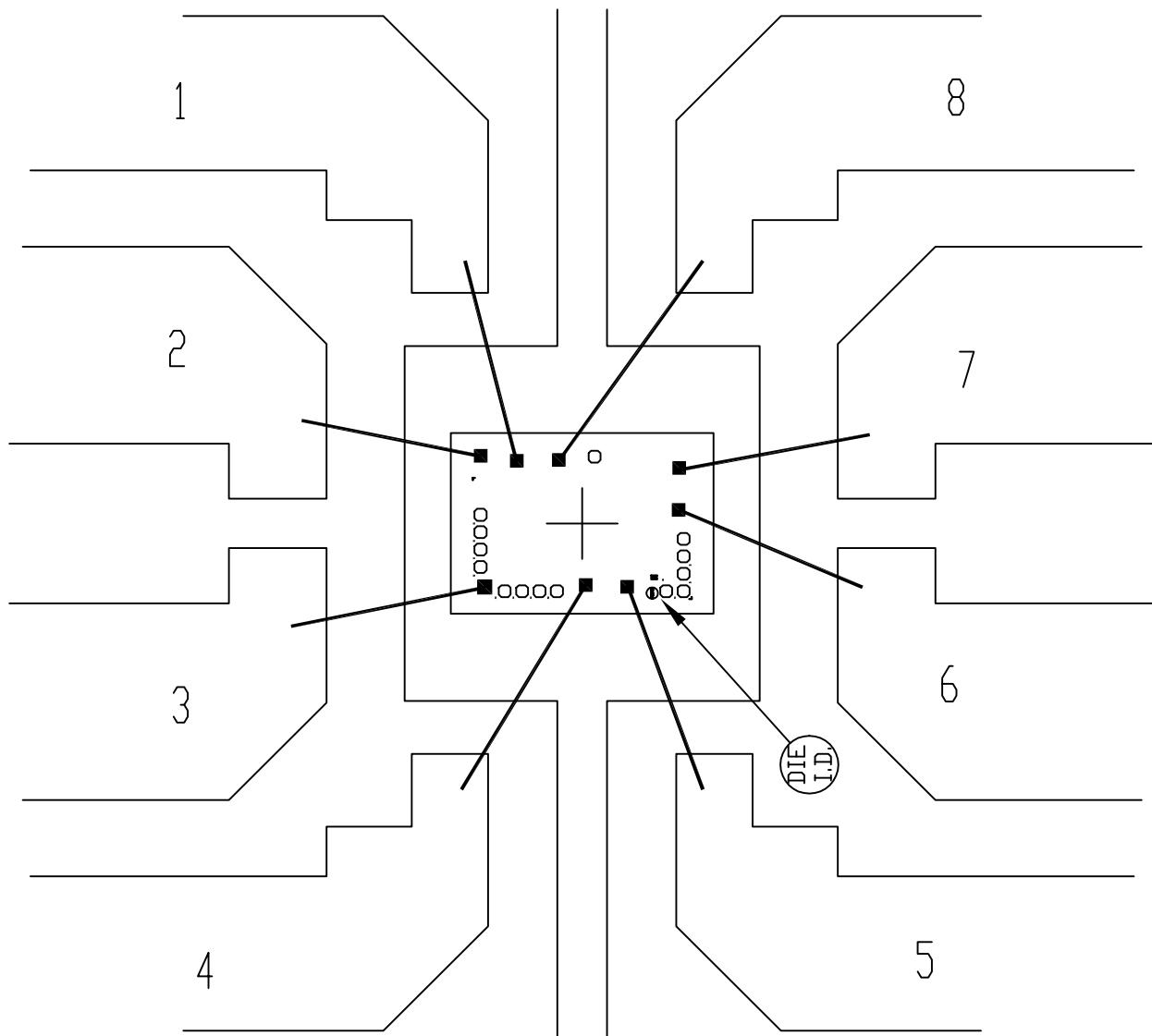




PKG. CODE:	U8-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE:	68x94	PKG. DESIGN			BOND DIAGRAM #: 05-1701-0164	REV: C



PKG. CODE:	S8-2		SIGNATURES	DATE	MAXIM	
CAV./PAD SIZE:	90 X 90	PKG. DESIGN			BOND DIAGRAM #: 05-1701-0101	REV: B



PKG. CODE:	P8-1		SIGNATURES	DATE	MAXIM	
CAV./PAD SIZE:	100 X 100	PKG. DESIGN			BOND DIAGRAM #:	REV: B
					05-1701-0100	

