



Integrated Device Technology, Inc.

FAST CMOS 16-BIT BIDIRECTIONAL 3.3V TO 5V TRANSLATOR

IDT54/74FCT164245T

FEATURES:

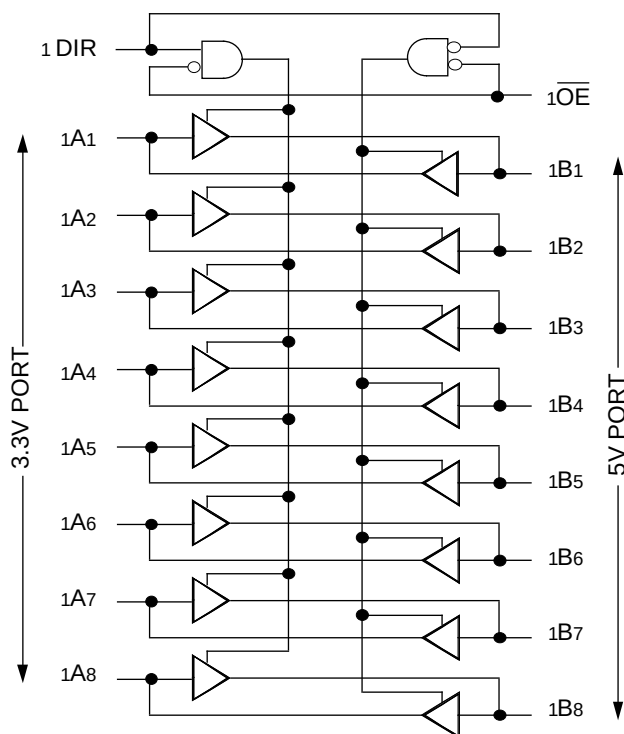
- 0.5 MICRON CMOS Technology
- Bidirectional interface between 3.3V and 5V busses
- Control inputs can be driven from either 3.3V or 5V circuits
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- 25 MIL Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- VCC1 = 5V ±10%, VCC2 = 2.7V to 3.6V
- High drive outputs (-32mA IOH, 64mA IOL) on 5V port
- Power-off disable on both ports permits "live insertion"
- Typical VOLP (Output Ground Bounce) < 0.9V at VCC1 = 5V, VCC2 = 3.3V, TA = 25°C

DESCRIPTION:

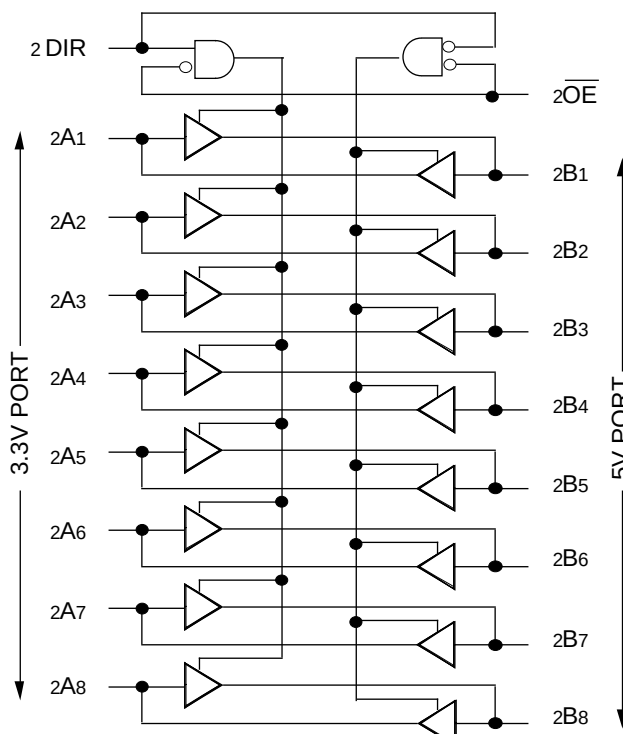
The FCT164245T 16-bit 3.3V-to-5V translator is built using advanced dual metal CMOS technology. This high-speed, low-power transceiver is designed to interface between a 3.3V bus and a 5V bus in a mixed 3.3V/5V supply environment. This enables system designers to interface TTL compatible 3.3V components with 5V components. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The A port interfaces with the 3.3V bus; the B port interfaces with the 5V bus. The direction control (xDIR) pin controls the direction of data flow. The output enable (xOE) overrides the direction control and disables both ports. These control signals can be driven from either 3.3V or 5V devices.

The FCT164245T is ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "hot insertion" of boards when used as backplane drivers. They also allow interface between a mixed supply system and external 5V peripherals.

FUNCTIONAL BLOCK DIAGRAM



2555 drw 01



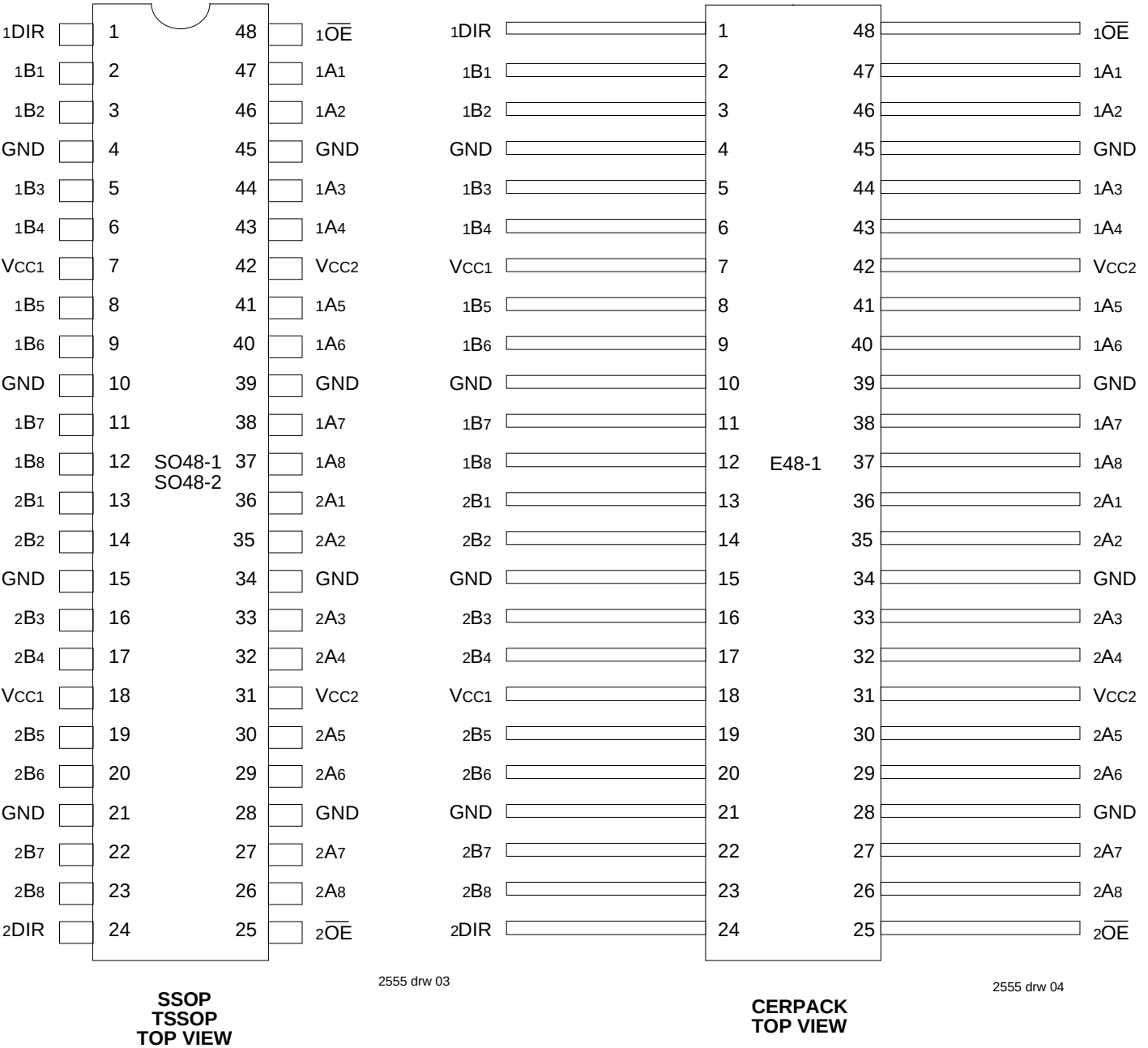
2555 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

FEBRUARY 1996

PIN CONFIGURATIONS



PIN DESCRIPTION

Pin Names	Description
$\overline{xOE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

2555 tbl 01

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
$\overline{xOE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

2555 tbl 03

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC1} +0.5	−0.5 to V _{CC1} +0.5	V
T _A	Operating Temperature	−40 to +85	−55 to +125	°C
T _{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T _{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	−60 to +120	−60 to +120	mA

2555 lmk 02

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except V_{CC2}.
- Power supply terminals V_{CC2}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	3.5	8.0	pF

NOTE:

- This parameter is measured at characterization but not tested.

2555 lmk 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT - 3.3V)

Following Conditions Apply Unless Otherwise Specified:

V_{CC1} = 5V ± 10%, V_{CC2} = 2.7V to 3.6V; Commercial: T_A = -40°C to +85°C, Military: T_A = -55°C to +125°C,

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	V _{CC1} = Max.	V _I = 5.5V	—	—	±5	μA
	Input HIGH Current (I/O pins)	V _{CC2} = Max.	V _I = V _{CC2}	—	—	±15	
I _{IL}	Input LOW Current (Input pins)		V _I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V _I = GND	—	—	±15	
V _{IK}	Clamp Diode Voltage	V _{CC2} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
V _{OH}	Output HIGH Voltage	V _{CC1} = V _{CC2} = Min.	I _{OH} = -0.1mA	V _{CC2} -0.2	—	—	V
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA MIL.	2.4	3.0	—	
		V _{CC2} = 3.0V V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4	3.0	—	
V _{OL}	Output LOW Voltage	V _{CC1} = Min.	I _{OL} = 0.1mA	—	—	0.2	V
		V _{CC2} = Min.	I _{OL} = 16mA	—	0.2	0.4	
		V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	—	0.3	0.55	
		V _{CC} = 3.0V V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	—	0.3	0.50	
I _{OFF}	Input/Output Power Off Leakage	V _{CC1} = 0V, V _{CC2} = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±100	μA
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC1} = Max., V _{CC2} = Max., V _O = GND ⁽³⁾		-70	-105	-150	mA
I _O	Output Drive Current	V _{CC1} = Max., V _{CC2} = Max., V _O = 1.5V ⁽³⁾		-40	-60	-90	mA
V _H	Input Hysteresis	—		—	150	—	mV
I _{CC2L} I _{CC2H} I _{CC2Z}	Quiescent Power Supply Current	V _{CC1} = Max., V _{IN} = GND or V _{CC2} V _{CC2} = Max.		—	0.35	2.0	mA

NOTES:

2555 tbl 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (B PORT - 5V)

Following Conditions Apply Unless Otherwise Specified:

VCC1 = 5V ± 10%, VCC2 = 2.7V to 3.6V; Commercial: TA = -40°C to +85°C, Military: TA = -55°C to +125°C,

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	VCC1 = Max.	V _I = VCC1	—	—	±5	μA
	Input HIGH Current (I/O pins)	VCC2 = Max.		—	—	±15	
I _{IL}	Input LOW Current (Input pins)		V _I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
V _{IK}	Clamp Diode Voltage	VCC1 = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
V _{OH}	Output HIGH Voltage	VCC1 = Min.	I _{OH} = -3mA	2.5	3.5	—	V
		VCC2 = Min.	I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.4	3.5	—	
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24mA MIL. I _{OH} = -32mA COM'L. ⁽⁵⁾	2.0	3.0	—	
V _{OL}	Output LOW Voltage	VCC1 = Min., VCC2 = Min.	I _{OL} = 48mA MIL. I _{OL} = 64mA COM'L.	—	0.2	0.55	V
		V _{IN} = V _{IH} or V _{IL}					
I _{OFF}	Input/Output Power Off Leakage	VCC1 = 0V, VCC2 = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±100	μA
I _{OS}	Short Circuit Current ⁽⁴⁾	VCC1 = Max., VCC2 = Max., V _O = GND ⁽³⁾		-80	-140	-225	mA
I _O	Output Drive Current	VCC1 = Max., VCC2 = Max., V _O = 2.5V ⁽³⁾		-50	-75	-180	mA
V _H	Input Hysteresis	—		—	150	—	mV
ICC1L ICC1H ICC1Z	Quiescent Power Supply Current	VCC1 = Max., V _{IN} = GND or VCC2 VCC2 = Max.		—	0.08	1.5	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC1 = 5.0V, VCC2 = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- Duration of the condition can not exceed one second.

2555 tbl 06

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC1} = \text{Max.}, V_{CC2} = \text{Max.},$ $V_{IN} = V_{CC2} - 0.6V^{(3)}$		—	12	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC1} = \text{Max.}, V_{CC2} = \text{Max.},$ Outputs Open $\overline{xOE} = xDIR = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC2}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A /$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC1} = \text{Max.}, V_{CC2} = \text{Max.},$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC2} - 0.6V$ $V_{IN} = \text{GND}$	—	1.2	4.7	mA
		$V_{CC1} = \text{Max.}, V_{CC2} = \text{Max.},$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC2} - 0.6V$ $V_{IN} = \text{GND}$	—	3.5	8.5 ⁽⁵⁾	

NOTES:

2555 tbl 07

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC1} = 5.0V$, $V_{CC2} = 3.3V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC1} + I_{CC2} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 I_{CC1} = Quiescent Current (I_{CC1L} , I_{CC1H} and I_{CC1Z})
 I_{CC2} = Quiescent Current (I_{CC2L} , I_{CC2H} and I_{CC2Z})
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	Com'l.		Mil.		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay A to B	CL = 50pF RL = 500Ω	1.5	5.0	—	—	ns
tPLH tPHL	Propagation Delay B to A		1.5	5.0	—	—	ns
tPZH tPZL	Output Enable Time xOE to B		1.5	6.5	—	—	ns
tPHZ tPLZ	Output Disable Time xOE to B		1.5	6.0	—	—	ns
tPZH tPZL	Output Enable Time xOE to A		1.5	6.5	—	—	ns
tPHZ tPLZ	Output Disable Time xOE to A		1.5	6.0	—	—	ns
tPZH tPZL	Output Enable Time xDIR to B ⁽³⁾		1.5	6.5	—	—	ns
tPHZ tPLZ	Output Disable Time xDIR to B ⁽³⁾		1.5	6.0	—	—	ns
tPZH tPZL	Output Enable Time xDIR to A ⁽³⁾		1.5	6.5	—	—	ns
tPHZ tPLZ	Output Disable Time xDIR to A ⁽³⁾		1.5	6.0	—	—	ns

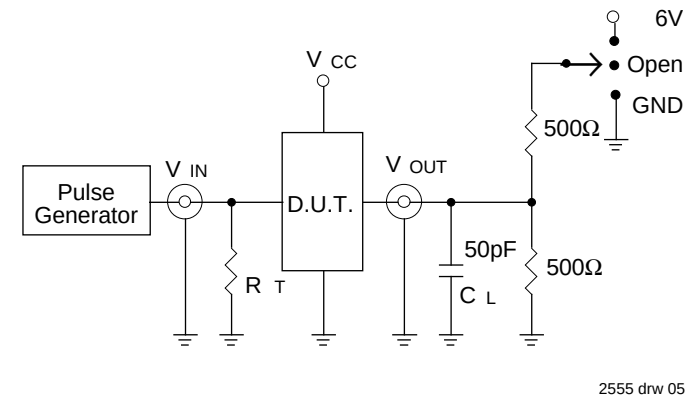
2555 tbl 08

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

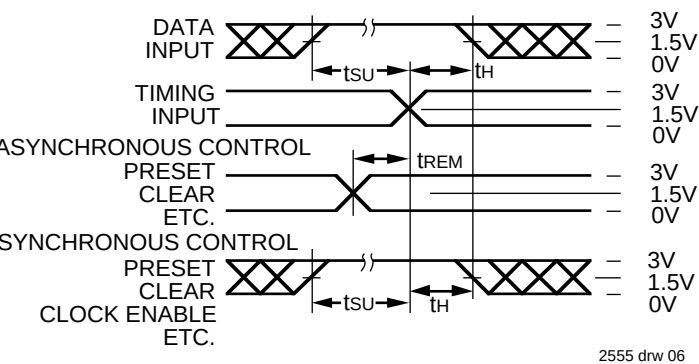


SWITCH POSITION

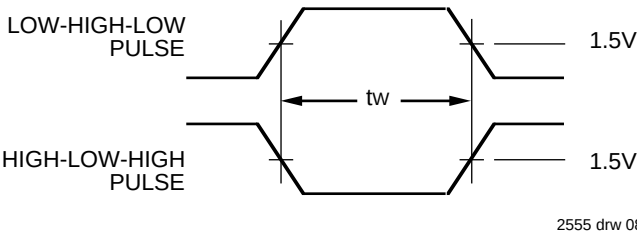
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS:
C_L= Load capacitance: includes jig and probe capacitance.
R_T= Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

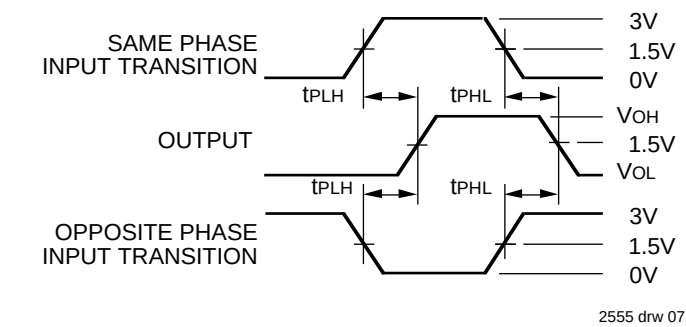
SET-UP, HOLD AND RELEASE TIMES



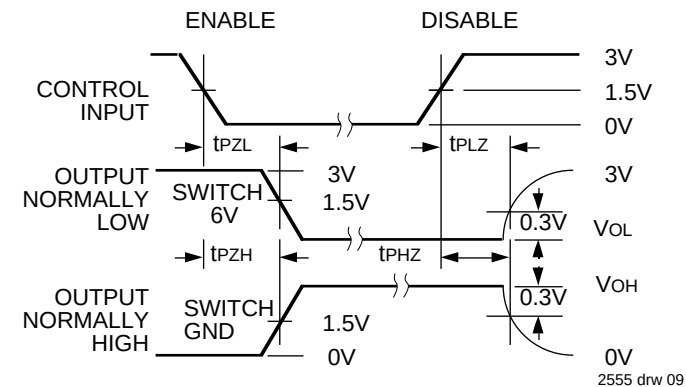
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



- NOTES:**
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
 - Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X	
	Temp. Range		Device Type	Package	Process	
					Blank B	Commercial MIL-STD-883, Class B
					PV PA E	Shrink Small Outline Package (SO48-1) Thin Shrink Small Outline Package(SO48-2) Cerpack (E48-1)
					164245T	Non-Inverting 16-Bit Bidirectional Translator
					54 74	−55°C to +125°C −40°C to +85°C

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